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(54) Multimedia graphics system.

(57) Bytes of different types of digital information, including standard interframe video (SIF), graphics, television and audio are transferred between a controller, storage memory and shift registers (e.g. FIFO's) individually associated with the different information types. For a VRAM memory, information is transferred in parallel, controlled by tag bus information, from the controller to the memory and then serially to the FIFO's, all at a frequency higher than a clock frequency in a monitor raster scan. The tag bus information is decoded and introduced to an additional FIFO. A state machine processes such additional FIFO information and transfers the digital information to the different FIFO's at times controlled in each line by such additional FIFO- e.g. particular times in each line for the SIF and graphics and thereafter, for television and audio, at times unrelated to any times in such line. The graphics transfer is timed to substantially fill, but not overflow, in such line the limited capacity of the associated FIFO. Their limited capacities cause the television and audio FIFO's to stop receiving bytes when filled to particular limits. For a DRAM memory, information is transferred, dependent upon the tag bus information, in parallel between the controller, memory and FIFO's at the clock frequency. In a "Rambus" system, a bus common with the controller, memory and FIFO's provides control and timing bytes. The information in successive bytes transferred through the common bus to the controller, memory and FIFO's dependent upon such timing and control information in such bytes.

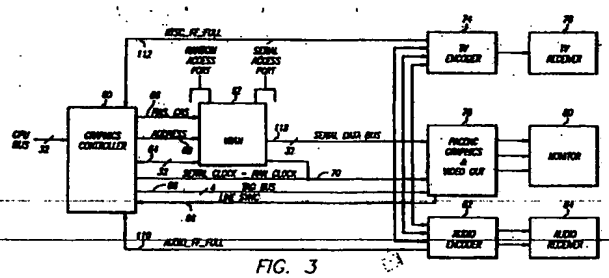

FIG. 3

EP 0 675 478 A1

This invention relates to apparatus for and methods of, processing digital information and more particularly relates to apparatus for, and methods of, processing different types of information in a multimedia environment. The invention especially relates to the selective processing of different types of information (including standard interframe video information, graphics information, television information and audio information) in an efficient and reliable manner.

Significant advances have been made in recent years in providing displays of a video information on a video monitor or screen. For example, graphics information has been displayed on a video monitor with enhanced resolution and fidelity as a result of significant advances in the processing of the digital information representing such colors and in the conversion of such digital information into an analog form. Such information has often been processed in digital form and thereafter converted to analog form in a personal computer or work station. In recent years, video information has been simultaneously displayed with the graphics information in such personal computers and work stations. For example, video information has been displayed in a window on the face of the video monitor of the personal computer or work station while graphics information has been displayed on the remainder of the monitor face.

In recent years there have also been significant strides in using miniaturized computers such as personal computers and work stations in processing information involving multimedia applications. These multimedia applications may take many different forms. For example, they may involve graphics, television, facsimile and/or audio. In spite of these advances, a suitable system does not exist which is sufficiently flexible to process different types of information efficiently, inexpensively and reliably. For example, the systems now in use are not capable of switching efficiently, inexpensively and reliably between different types of presentations such as graphics, video and audio. This has been particularly true when information from more than one type of media (e.g. graphics, video, television and audio) is to be presented simultaneously. This has limited the utility of the systems now in use. Such limitations exist now in multimedia equipment even though considerable amounts of money have been expended, and considerable effort has been devoted, through the years, and particularly in recent years, to develop a satisfactory multimedia system.

In one embodiment of this invention, bytes of different types of digital information including standard interframe video (SIF), graphics, television and audio are transferred between a controller, a storage memory and shift registers (e.g. FIFO's) individually associated with the different information types. For a VRAM memory, information is transferred in parallel, controlled by tag bus information, from the controller to the memory and then serially from the memory to the FIFO's, all at a frequency higher than a clock frequency in a monitor raster scan.

The tag bus information is decoded and introduced to an additional FIFO. A state machine processes such additional FIFO information and transfers the digital information to the different FIFO's at times controlled in each line by such additional FIFO-e.g. particular times in each line for the SIF and the graphics and thereafter, for television and audio, at times unrelated to any times in such line.

The graphics transfer is timed to substantially fill, but not overflow, the limited capacity of the associated FIFO in each line. Their limited capacities cause the television and audio FIFO's to stop receiving bytes when filled to particular limits. For a DRAM memory, information is transferred, dependent upon tag bus information, in parallel between the controller, memory and FIFO's at the clock frequency. In a "Rambus" system, a bus common with the controller, memory and FIFO's provides control and timing bytes. The information in successive bytes is transferred through the common bus to the controller, memory and FIFO's dependent upon such timing and control information in such bytes.

In the drawings:

Figure 1 is a schematic block diagram of a system of the prior art;

Figure 1(a) shows wave forms at strategic terminals in the system shown in Figure 1;

Figure 2 is a schematic block diagram of another system of the prior art, this system being shown and disclosed in a patent application recently filed in the Patent Office by the assignee of record in this application;

Figure 2(a) shows wave forms at strategic terminals in the system shown in Figure 2;

Figure 3 is a schematic block diagram of a system constituting one embodiment of the invention;

Figure 3(a) shows waveforms at strategic terminals in the system shown in Figure 3;

Figure 4 is a table illustrating the different types of digital information processed by the system shown in Figure 3;

Figure 5 illustrates the sequence of signals processed by the system of Figure 3 in each line in a raster scan in a monitor included in Figure 3;

Figure 5(a) illustrates wave forms at strategic terminals in the system of Figure 3;

Figure 6 is an expanded schematic block diagram illustrating one of the blocks in Figure 3 in additional detail;

Figure 7 is an expanded schematic block diagram illustrating one of the blocks in Figure 6 in additional detail;

Figure 8 is a schematic block diagram of another embodiment of the invention;

Figure 9 is a schematic block diagram of a further embodiment of the invention; and

Figure 10 is an expanded schematic block diagram illustrating one of the blocks in Figure 9 in additional detail.

Figure 1 illustrates an embodiment of the prior art. The embodiment includes a graphics controller 10, a storage memory such as a VRAM 12 and stages 14 comprising a random access memory (RAM) and a digital-to-analog converter (DAC). The graphics controller 10 may be a central processing unit which transfers information into the VRAM 12 as indicated at 16. Information is in turn transferred from the VRAM 12 into the stages 14 (designated as "RAMDAC" in Figure as an acronym for random access memory and digital-to-analog converter). The random access memory may comprise a palette (also known as a look-up table) which is well known in the art. The transfer of information into the RAMDAC 14 is indicated at 18. A "/32" indication is provided adjacent the line 18 to indicate that there may be thirty two (32) bits in each byte of information. The analog output from the RAMDAC is indicated at 19. This output may be introduced to a monitor 20 for display on the face of a display screen in the monitor.

The palette in the RAMDAC may have a plurality of positions each indicating an individual color. The color at each position may be indicated by a first plurality of bits indicating the primary color red, a second plurality of bits indicating the primary color blue and a third plurality of colors indicating the primary color green. When an individual position in the palette is selected, the bits indicating each of the primary colors are converted to corresponding analog values in the RAMDAC. The respective intensities of the three primary colors at each pixel position controls the color generated at such pixel position on the face of the monitor 20.

The graphics controller 10 introduces binary indications into successive positions in the VRAM 12. Each of these binary indication is comprised of a plurality of binary bits. Each plurality indicates a particular position to be selected in the palette. The information transferred from the graphics controller 10 to the VRAM 12 and from the VRAM to the RAMDAC 16 may be provided at a particular clock frequency as indicated by a line 22 extending from the graphics controller 10 to the VRAM 12 and the RAMDAC 14.

Graphics information may be displayed on the screen of the monitor 20. When the RAMDAC is included in a work station (not shown), the image on the face of the monitor 20 may be formed by a plurality of pixels in a raster scan. For example, twelve hundred and eighty (1280) pixels may be provided in each horizontal line in the raster scan and ten hundred and twenty four(1024) lines may be provided in such raster scan. The raster may be refreshed at a rate of seventy hertz (70 Hz). Under such circumstances, the pixels are presented at a frequency of one hundred and thirty two megahertz (132 Mhz). When the VRAM is thirty two (32) bits wide, four (4) words each of eight (8) bits may be presented in parallel. This allows the information to be transferred serially from the VRAM at a frequency of thirty three megahertz (33 Mhz). Since each word comprises eight (8) bits, the palette may have two hundred and fifty six (256) different positions each indicating an individual color.

It may be desired to update the palette in the RAMDAC 14. This may be accomplished during the horizontal retrace period at the end of each line or during the horizontal blanking interval at the beginning of each line. The horizontal retrace period is relatively short but the horizontal blanking interval in each line is approximately twelve percent (12%) of the duration of the line. The palette may also be updated during the vertical retrace period at the end of each raster scan. The vertical retrace period is considerably longer than each horizontal retrace period. Figure 1 (a) schematically indicates the clock signals on the line 22 as at 24 and schematically indicates the blanking interval 26 at the beginning of each line.

The system shown schematically in Figure 1 and discussed above has had extensive usage in the prior art. It is advantageous in that it is relatively simple and reliable. It is disadvantageous in that it provides only a limited number of pseudo colors rather than real colors. Furthermore, it is able to provide only graphics information for display on the monitor 20. It is also not capable of fully utilizing the advantages offered by the latest models of VRAMS which are just being introduced to the market. These VRAMS are capable of operating at a frequency of sixty six megahertz (66 Mhz). This is in contrast to the maximum frequency response of thirty three megahertz (33 Mhz) for the VRAMs now on the market.

Figure 2 schematically shows a system which is disclosed and claimed in application Serial No. 08/014,359 (file D-2657) filed by Jonathan I. Siann, Conrad M. Coffey and Jeffrey L. Easley on February 5, 1993, for a "System For, and Method of, Displaying Information from a Graphics Memory and a Video Memory on a Display Monitor" and assigned of record to the assignee of record of this application. A graphics controller 40, a storage member (such as a VRAM 42) and stages 44 are included in the system. The stages 44 may include

a shift register such as a first-in-first-out (FIFO) register and may also include a random access memory (RAM) and a digital-to-analog converter (DAC).

Information is introduced into the VRAM 42 from the graphics controller 40 in the embodiment shown in Figure 2. This information may be graphics information in a first portion 42a of the VRAM and may also be standard interframe video information (SIF) such as NTSC or PAL video in a second portion 42b of the VRAM. The first and second portions of the VRAM are indicated schematically by a broken horizontal line in the VRAM 42. This information may illustratively have 320 pixels per horizontal line and may have 240 horizontal lines in each raster scan. The graphics information for a frame may be stored in one portion of the VRAM 42 as indicated at 42a and the standard interframe video information for a frame may be stored in a second portion 42b of the VRAM. This is advantageous over the prior art because it eliminates the need for a separate storage memory to store the standard interframe video information. The graphics information and the standard interframe video information are transferred from the graphics controller 40 into the VRAM 42 in parallel form. Each byte of parallel information may have thirty two (32) bits.

The graphics information and the standard interframe video information are serially transferred from the VRAM 42. The graphics information in the portion 42a of the VRAM 42 is transferred, as in the embodiment shown in Figure 1, at a rate of thirty three megahertz (33 Mhz) by providing four (4) words, each of eight (8) bits. The transfer is made into the RAMDAC portion of the stages 42 in a manner similar to that disclosed above for the embodiment shown in Figure 1. This transfer occurs during the portion of each line in the raster scan in a monitor 46 other than the video blanking interval. This transfer is in synchronism with the rate of presentation of pixels on the screen of the video monitor 46. The transfer is accordingly at thirty three megahertz (33 Mhz). This transfer is indicated at 48a in Figure 2a.

However, as previously indicated, the VRAMs now being introduced into the market can transfer information serially out of the VRAM 42 at a rate of sixty six megahertz (66 Mhz). The transfer accordingly does not utilize the full capability of the VRAM 42. During the horizontal retrace and the horizontal blanking interval in each line in the raster scan in the monitor 46, the standard video information (SIF) is transferred serially from the portion 42b of the VRAM 42 into the FIFO portion of the stages 44 at a frequency of sixty six megaherts (66 Mhz). This transfer is indicated at 48b in Figure 2a.

The horizontal blanking interval constitutes only about twelve percent (12%) of the time in a line. However, since there are only three hundred and twenty (320) pixels in a line in standard interframe video information, the horizontal retrace period and the horizontal blanking interval are sufficiently long to transfer all of the standard interframe video information for a line into the FIFO portion of the stages 44. This is particularly true if the information transfer is at a rate of sixty six megahertz (66 Mhz). The information stored in the FIFO portion of the stages 44 for each line is converted into a line of twelve hundred and eighty (1280) pixels in the stages 44 by techniques known in the prior art. A multiplexer included in the stages 44 (but not specifically shown) then selects, in accordance with information from the controller 40, whether the graphics information in the RAM or the standard interframe information obtained from the FIFO will be converted by the DAC to analog information for display on the screen of the monitor 46. The video information in the portion 42b of the VRAM is transferred into the stages 44 at the graphics frequency of thirty three megahertz (33 Mhz).

The system shown in Figure 2 and described above has certain important advantages. As described above, it uses only one (1) VRAM to store two (2) types (graphics and standard interframe video) information. It provides for the transfer of both types of information in each line in the raster scan and provides for the display of both types of information simultaneously in the successive frames on the screen of the monitor 46. For example, the graphics information may be displayed in the major portion of the raster scan and the standard interframe video information may be displayed in a window in the raster scan. However, the full transfer capabilities of the VRAM at sixty six megahertz (66 Mhz) are utilized for only a small (12%) portion of each line. Furthermore, only two (2) types of information can be presented. This is less than the number of different types of information that it is often desired to provide in a multimedia system.

Figure 3 is a schematic diagram illustrating one embodiment of the invention. This embodiment includes a graphics controller 60 similar to that shown in Figures 1 and 2. Bytes of digital information are transferred from the graphics controller 60 to a storage member such as a VRAM 62 similar to that shown in Figures 1 and 2. Each byte may be thirty two (32) bits wide and may be provided through a bus 64. Each byte is transferred to a particular location in the VRAM 62 under the control of address information passing to the VRAM 62 through a pair of lines 66 and 68. A row address select (RAS) may be provided on the line 66 and a column address select (CAS) may be provided on

the line 66. The digital information passing through the lines 64, 66 and 68 may be at the VRAM clock frequency of sixty six megahertz (66 Mhz). These clock signals are provided through a line 70.

The digital information in the VRAM 62 is transferred from the VRAM serially at the clock frequency of sixty six megahertz (66 Mhz). Unlike the embodiment shown in Figure 2 in which this high clock rate was possible only during the blanking interval in each horizontal line in the raster scan, the high clock rate is essentially continuous in the embodiment shown in Figure 3. The only time that the clock is not at sixty six megahertz (66 Mhz) is when a serial register transfer is being made inside the VRAM at the request of the graphics controller 60. During this time, new data is being transferred from the storage location in the VRAM register to the VRAM serial data register. This occurs for only a few cycles of the clock frequency in each line in the raster scan.

The blanking interval in each line in the raster scan is indicated at 70 in Figure 3(a). The serial transfer of data from the VRAM 62 at essentially the clock frequency of sixty six megahertz (66 Mhz) is indicated at 72 in Figure 3(a). The information transferred serially from the VRAM 72 at this clock frequency may represent a number of different media. For example, the information may constitute television information in NTSC, PAL or SECAM form. This information is transferred to a television encoder 74 and is then transferred from the television encoder to a television receiver 76.

The digital information may also be transferred from the VRAM 62 to stages 78. This information may have several different forms. It may constitute standard interframe video information (SIF). Actually, the standard interframe video interframe information may have several different forms. For example, SIF information may have 240 lines each of 320 pixels in a raster scan (designated as SIF1). Similarly, information designated as SIF2 may have 120 lines and 160 pixels in each line.

The digital information transferred from the VRAM 62 may also be in graphics form. The graphics information may have several different formats. For example, when the graphics information is intended for a workstation, there may be 1024 rows and 1280 pixels in each row. When the graphics information is intended for a VGA format, there may be 4xx rows and 6xx pixels in each row. For a super VGA format, the number of rows may be 768 and the number of pixels in each row may be 1024. The stages 78 may receive other types of information in addition to the standard interframe video information and the graphics information. For example, digital information may be transferred from the VRAM 62 to the stages 78 to indicate cursor information.

The information transferred to the stages 78 is introduced to a monitor 80 corresponding to the monitors 20 and 46 respectively shown in Figures 1 and 2. Audio information may also be transferred to an audio encoder 82 for storage and conversion to analog form and may then be transferred from these stages to an audio receiver 84. As will be appreciated and as will be seen from subsequent Figures, the stages 78 are shown in simplified form as a single stage but may actually constitute a plurality of different stages.

Some control may accordingly have to be provided to direct the information from the VRAM 62 at different times to individual ones of the television encoder 74, the stages 78 (including standard interframe video, graphics and cursor encoders) and the audio encoder 82. This control is provided by a tag bus 86 which may provide four (4) bits in parallel. In the embodiment shown in Figure 3, the tag bus 86 provides these four (4) bits for each byte or packet of thirty two (32) bits from the VRAM 62. The four (4) bits are encoded to direct such byte or packet into the proper one of the different encoders. A line 88 also extends in Figure 3 from the stages 78 to the graphics controller 60 to synchronize the operation of the graphics controller in each line in the raster scan in providing for the passage of information serially from the VRAM 62 to the different encoders in the stages 78.

As illustrated in Figure 4 and as discussed above, different types of digital information may be transferred from the VRAM 62 to the different types of encoders shown schematically in Figure 3 and in additional detail in Figure 6. Such different types of digital information may include graphics, different types of standard interframe video (such as those designated as SIF1 and SIF2), audio, television (designated as NTSC only be way of illustration) and cursor.

The information transferred from the VRAM 62 may also include what is designated in Figure 4 as a palette shadow. This information involves an updating of every position in the palette or look-up table at the end of each frame in the raster scan in the monitor 80 in Figure 3. The updating is provided in each position in the palette even though the color information in some positions in the palette remains unchanged. This is different from the updating provided in the prior art. In the prior art, the updating is generally provided at the end of each line and is only in selected positions. The updating of all of the positions in the palette at the end of each frame in the raster scan may be provided because the updating is occurring at the high frequency of sixty six (66) megahertz.

The transfer of information from the VRAM 62 may occur in a particular sequence in each line in

the raster scan in the monitor 80. This sequence is illustratively shown in Figure 5. The sequence in each line may be as follows: standard interframe video information (SIFI and SIF2), graphics information, audio information and television information (designated as NTSC). The standard interframe video information and the graphics information may be synchronized at a particular time in each line. The audio information and the television (NTSC) information may occur after the standard interframe video information and the graphics information in each line but at a time unrelated to any synchronizing information, such as the blanking interval, in such line. It will be appreciated that, although NTSC information is specifically designated in Figure 5, other types of television information such as PAL or SECAM are within the scope of the invention.

Figure 5 illustrates the sequence of the different types of digital information in each line. As will be seen, the standard interframe video information (SIF1 and SIF2) occurs first in each line. This is followed by the graphics information. The audio and television (e.g. NTSC) information then occur in each line. For the line in each raster scan where the cursor appears, the cursor information occurs after the television (e.g. NTSC) information. During the vertical retrace interval in each raster scan, the palette shadow information is provided to update the palette or look-up table for the graphics information in the next raster scan.

As shown in Figure 5, the graphics data is transferred into a shift register such as a first-in-first out register 100 (e.g. FIFO) in Figure 6. The FIFO 100 and other FIFO's in the embodiment shown in Figure 6 and in other Figures in this application are well known in the art. They receive and store bytes of information. These bytes of information are shifted through the FIFO 100 (and other FIFO's) in the same order as they are received. When the information introduced into the FIFO 100 has been shifted through the FIFO, the bytes of digital information are then transferred from the FIFO in the same order that they are received.

The FIFO 100 for the graphics information has a capacity less than the number of pixels in each line. This causes the transfer of the bytes of binary graphics information into the FIFO 100 to be initiated at a particular instant in each line in the raster scan. This initiation of the transfer of the digital graphics information in each line into the FIFO 100 occurs at a particular time during the blanking interval 102 (see Figure 5) in each line. By initiating the transfer of the digital graphics information into the FIFO 100 at such time, substantially the full capacity of the FIFO 100 can be utilized in receiving the bytes of graphics information for the line without any of the graphics information being unable to be transferred into the FIFO because the FIFO has become filled. Furthermore, with this type of transfer, substantially the full capacity of the FIFO is used all of the time.

The standard interframe video information is transferred into storage registers such as FIFO's 104 (for the SIF1) and 106 (for the SIF2) in Figure 6. The transfer of the standard interframe video information into the FIFO's 104 and 106 for each line may be initiated at a time 108 in Figure 5 before the blanking interval for the line. The FIFO's 104 and 106 may have a full capacity (rather than a partial capacity as for the FIFO 100) because the capacities of the FIFO's 104 and 106 are not very large. This results from the fact that there are only 320 pixels per line in SIF1 information and only 160 pixels per line in SIF2 information. This is in contrast to 1280 pixels per line in graphics information for display on the monitors in work stations.

As will be seen from Figure 5 and from the discussion above, the transfers of the standard interframe video information and the graphics information may be initiated at particular times in each line in the raster scan in the monitor 80 in Figure 3. The transfer of the audio information for each line in the raster scan into the audio encoder 82 in Figure 3 may be initiated immediately after the transfer of the graphics information for that line has been completed. However, the transfer of the audio information may be initiated without reference to any particular time in each line. The capacity of the audio encoder 82 (which may be a FIFO) is somewhat limited. Because of this, when the audio encoder 82 has been substantially filled in a line, it sends a signal (designated as "Audio FF Full") on a line 110 in Figure 3 to the graphics controller 60. This signal causes the graphics controller 60 to instruct the VRAM 62 to stop sending bytes of digital audio information to the audio encoder 82 for that line.

In like manner, the transfer of the bytes of the digital television information may be initiated in each line after the transfer of the audio information in that line. The transfer of such bytes of digital television information in each line is made into the encoder 74 in Figure 3. As with the audio information, the transfer may be made on any asynchronous basis in each line, in other words, without reference to any particular time in such line. The capacity of the encoder 74 may be somewhat limited. Because of this, the encoder sends a signal through a line 112 in Figure 3 to have the graphics controller 60 discontinue the transfer of television information into the encoder 74 from the VRAM 62 in any line when the encoder has been filled to a particular capacity in that line. This signal is designated in Figure 3 as "NTSC-FF-FULL".

The stages 78 in Figure 3 are shown in additional detail in Figure 6. This is indicated by broken lines which extend around the stages shown in Figure 6 and which have the numerical designation 78. As previously described, the stages 78 in Figure 3 may include the stages 100, 104 and 106 in Figure 6. They may also include FIFO's 114 and 116 in Figure 6. The FIFO 116 receives the cursor information in a particular line in the raster scan. The stages 100, 104, 106 and 116 may receive bytes of digital information through a line 118 (also shown in Figure 3) from the VRAM 62. In contrast, the FIFO 114 may receive the timing and control information from the tag bus 84 also shown in Figure 3.

The information from the tag bus 84 may pass through an amplifier 120 in Figure 6 to decoders 122, 124, 126 ,128 and 130 respectively for the FIFO's 104, 106, 100, 114 and 116. Decoders such as the decoders 122, 124, 126, 128 and 130 are well known in the art. They decode the four (4) bits of digital information in the tag bus 84 for each byte of digital information in the bus 118. The decoded information controls which one of the FIFO's 100, 104, 106 and 116 will receive and store that byte of information. Furthermore, the decoder 128 decodes the bytes of the digital information in the tag bus 84 to provide timing and control information in binary form. This timing and control information passes from the decoder 128 into the FIFO 114.

The information in the FIFO 114 then passes into a timing state machine 134 which processes this information to produce various timing and control signals for each line in the raster scan. For example, the timing state machine 134 may produce the synchronizing signal on the line 88 to initiate the transfer of the standard interframe video information in each line into the FIFO's 104 and 106 at the time indicated at 108 in Figure 5(a). The timing state machine 134 may also produce on a line 136 the horizontal sync signal for each line in the raster scan and on a line 138 the vertical sync signal after each such raster scan. The timing state machine may also produce the horizontal blanking signal (see 70 in Figure 3a and 102 in Figure 5) on a line 154 in Figure 6.

The timing state machine 134 may also produce signals on a line 135 for introduction to the FIFO's 100, 104, 106 and 116. These signals may activate individual ones of the FIFO's 100, 104, 106 and 116 to provide for the passage of signals from these FIFO's at times determined by the timing state machine. The signals from the standard interframe video FIFO's 104 and 106 pass to a scaler 144; the signals from the graphics FIFO pass to a palette 146; and the signals from the cursor FIFO 116 pass to a cursor palette 147.

The timing state machine 134 may additionally produce a priority signal on a line 140. This signal is introduced to a pixel priority multiplexer 142 to control whether the standard interframe video information from one of the FIFO's 104 and 106 or the graphics information from the FIFO 100 will pass through the multiplexer at each instant. The information in the FIFO's 104 and 106 may be initially introduced to the scaler 144 and the scaled information may be then passed to the multiplexer 142. The scaler 144 is well known in the art and different examples of the scaler 144 are disclosed in some detail in co-pending application Serial No. 08/014,359 (attorneys file D-2657). The scaler increases the number of bytes in the FIFO's 104 and 106 for each line in the raster scan into a number of bytes corresponding to the number of bytes in each line in the graphics information.

The bytes of the digital information in the FIFO 100 for each line may be introduced to the palette 146 to select the individual positions in the palette for the passage of color information to the pixel priority multiplexer 142. The palette 146 corresponds in construction to the palette in the RAM-DAC 14 in Figure 1 and to the palette in the stages 44 in Figure 2. In like manner, the FIFO 116 passes information to the cursor palette 147 which passes the cursor information to the multiplexer 142 for passage through the multiplexer. The passage of the cursor information from the palette 147 through the multiplexer 142 may be controlled by the priority signal on the line 140.

The bytes of information passing through the multiplexer 142 from the scaler 144, the palette 146 and the palette 147 may be introduced to digital-to-analog converters 148, 150 and 152 respectively for the primary colors red, green and blue. The analog signals from the converters 148, 150 and 152 then pass to the monitor 80 shown in Figure 3. The converters 148, 150 and 152 may receive a blanking signal on the line 154 from the timing state machine 134. The blanking signal blanks the converters 148, 150 and 152 during each line in the raster scan.

The timing state machine 134 is shown in additional detail in Figure 7 as being included within broken lines designated as 134. As shown in Figure 7, each byte of information from the timing FIFO 114 may comprise thirty two (32) bits. Of these, twenty (20) bits may be introduced to stages 160 (designated as "state") which produce the horizontal sync signal on the line 136, the vertical sync signal on the line 138, the blanking signal on the line 154, the priority signal on the line 140 and the signals on the lines 135 to the FIFO's 100, 104, 106 and 116. The timing of these signals is provided by the other twelve (12) bits in each byte from the timing FIFO 114. These bits are intro-

duced to a counter 162 which is preset to a particular value. The counter 162 then counts downwardly by an integer through a documenting stage 164 every time that a pixel clock signal is produced on the line 70 (also shown in Figure 3). When the counter 162 reaches a count of zero (0), the count from the counter corresponds to a count preset in a comparator 166. The comparator 166 then produces a signal on a line 168 to provide for the passage of the next byte of thirty two (32) bits from the FIFO 114 to the stages 160 and the counter 162.

Figure 8 schematically illustrates an embodiment in which a dynamic random access memory (DRAM) 170 may be used instead of a VRAM as in the previous embodiment. The DRAM 170 is advantageous because the cost of a DRAM is approximately one half (1/2) of the cost of a VRAM of the same size. The embodiment shown in Figure 8 is also advantageous because all of the transfer of information, even from the DRAM 170, to PACDAC stages 172 is in parallel. This tends to increase the speed of operation of the system shown in Figure 8.

However, a DRAM is disadvantageous in comparison to a VRAM because first information cannot be simultaneously introduced into a DRAM while second information is being transferred out of the DRAM. Furthermore, the data bandwidth of the system shown in Figure 8 is not as great as that of Figure 3 because only the random access port of the DRAM 170 is used and the bandwidth of the DRAM is typically less than half of the sixty six megahertz (66 Mhz) bandwidth in the VRAMs which are being introduced into the market.

The embodiment shown in Figure 8 includes a graphics controller 172 similar to the graphics controller 60 shown in Figure 3. It also includes stages 174 designated as "PACDAC". These stages correspond to the stages 78 shown in Figure 3. One difference between the system shown in Figure 8 and the system shown in Figure 3 is that, in the system shown in Figure 8, each of the controller 172, the DRAM 170 and the PACDAC stages 174 can communicate with the others. The transfer of information into the DRAM 170 from the controller 172 and out of the DRAM 172 is controlled by address signals on a bus 175. The signals on the bus 175 correspond to the signals on the lines 66 and 68 in Figure 3.

As in the embodiment shown in Figure 3, a tag bus 176 is provided in Figure 8 to control the destination of the bytes of the different types of information in the DRAM 170 and the time in each line for the transfer of such bytes. As in the embodiment shown in Figure 3, the PACDAC stages 174 can have the construction shown in Figure 6 and the timing state machine can have the construction shown in Figure 7. The different types of information can be provided in the sequence shown in Figure 5 and the timing for the standard interframe video information in each line can be provided as by a pulse on a line 175 corresponding to the pulse 108 in Figure 5.

As shown in Figure 8, the bytes of digital information transferred between the DRAM 170, the graphics controller 172 and the PACDAC stages 174 on a bus 177 may have sixty four (64) bits. The DRAM 170 may accordingly be formed from four (4) DRAMs in parallel, each DRAM having sixteen (16) bits. As in the embodiment shown in Figure 3, the FIFO for the graphics information may have a limited capacity to conserve cost and space. The FIFO's for the television (e.g. NTSC) and audio information may also have limited capacities as in the embodiment shown in Figure 3. This is indicated by the designation of "NTSC-FF-FULL" for a line 178 and "AUDIO-FF-FULL" for a line 180. Signals may accordingly be produced respectively on the lines 178 and 180 to instruct the graphics controller to interrupt the transfer of information from the DRAM 170 into the television and audio FIFO's when these FIFO's become filled to a particular limit. Clock signals may be produced on a line 182 in the embodiment shown in Figure 8 in a manner similar to the production of clock signals on the line 70 in the embodiment shown in Figure 3.

The embodiment shown in Figure 9 is intended to be used for a system designated as "RAMBUS." The "RAMBUS" system is well known in the prior art. For example, International application PCT/US91/02590 was published on October 31, 1991. The embodiment shown in Figure 9 represents an improvement in the "RAMBUS" system of the prior art. The system shown in Figure 9A includes a graphics controller 190, PACDAC stages 192 and DRAMs 194 as in the embodiments shown in Figures 3 and 8. However, unlike the embodiments shown in Figures 3 and 8, the controller 190, the stages 192 and the DRAMs 194 may be connected by a common bus 196. Packets or bytes of digital information may pass through the bus 196 between the controller 190, the stages 192 and the DRAMs 194. Each of these bytes or packets may have ten (10) bits.

Eight (8) of the ten (10) bits in each byte or packet in the embodiment of Figure 9 may comprise data. The other two (2) bits in each byte or packet may be used to provide parity checking and to provide special signalling. The two (2) bits for special signalling in individual ones of the bytes or packets may be used to indicate that the eight (8) data bits in such bytes or packets provide the information provided in the Tag Bus in the embodiments shown in Figures 3 and 8. For example,

such eight (8) bits specify the destination of the data in the subsequent bytes or packets and specify the timing for the information in the subsequent bytes or packets.

The graphics controller 190 in Figure 9 may have the same construction as the graphics controller in the embodiments shown in Figures 3 and 8. The DRAMs 194 in the embodiment of Figure 9 may have the same construction as the DRAM 170 in the embodiment shown in Figure 8. However, the DRAMs 190 may be only ten (10) bits wide rather than sixty four (64) bits wide as in the embodiment shown in Figure 8. The PACDAC stages 192 shown in Figure 9 are substantially the same as the PACDAC stages shown in Figure 3 except that, as described above, a Tag Bus is not included in the embodiment shown in Figure 9. Because of this, the PACDAC stages 192 may have the construction shown in Figure 10. They are included within broken lines designated as 192 in Figure 10. In the PACDAC stages shown in Figure 10, different stages have the same numerical designation as the stages shown in Figure 6 except that they are preceded by the numeral "2" rather than the numeral "1" as in the embodiment shown in Figure 6. For example, the graphics FIFO is designated as "200" in Figure 10 but is designated as "100" in Figure 6.

In the embodiment shown in Figure 10, the bytes or packets on the bus 196 from the graphics controller 190 may pass to the decoder 228 which decodes the bits indicating that the eight (8) data bits in the bytes or packets contain timing and control information rather than digital information for the other FIFO's. These eight (8) bits in the timing and control packets may then pass to the timing FIFO 214. The eight (8) bits may then pass from the FIFO 214 to the timing state machine 234 which produces the timing and control signals indicating the destination of the subsequent bytes or packets of information. The destination signals may be produced by the timing state machine 234 on lines 235. These signals may accordingly activate one of the decoders 222, 224, 226 and 230. The activated one of the decoders 222, 224, 226 and 230 may then pass the subsequent bytes or packets of information on the line 218 to the respective ones of the FIFO's 200, 204, 206 and 216.

When the standard interframe video signals pass through one of the video FIFO's 204 and 206, the scaler 244 acts on these signals to scale the number of pixels in each line upwardly and the signals from the scaler 244 may then pass to the pixel priority multiplexer 242. This is the same as in the embodiment shown in Figure 6. As in the embodiment shown in Figure 6, the signals from the graphics FIFO 200 may select positions in the palette 246 and these signals may pass to the pixel priority multiplexer 242. Similarly, the signals in the FIFO 216 may select positions in the cursor palette 246 and the signals from the palette may pass to the pixel priority multiplexer 242.

The pixel priority multiplexer 242 may pass the signals from individual ones of the scaler 244, the palette 246 and the cursor FIFO 216 in accordance with signals on the line 240 from the timing state machine 234. The signals passing through the pixel priority multiplexer 242 are introduced to the color converters 248, 250 and 252. The passage of the signals from the converters 248, 250 and 252 and the display of the signals on the monitor 280 are controlled by signals produced on the lines 236, 238 and 254 by the timing state machine 234.

The apparatus disclosed above has several important advantages. It provides for an efficient processing of different types of information including standard interframe video information, graphics information, television information, audio information and cursor information. The system provides for such processing either with a VRAM or a DRAM. In some embodiments, the system employs a data bus for the different types of information and employs a tag bus for the timing and control information. For the RAMBUS embodiment, the system employs a common bus for all of the sub-systems in the system and uses individual bits in each byte or packet on such bus to indicate whether the data bits in such byte or packet represent media information or timing and control information.

Although this invention has been disclosed and illustrated with reference to particular embodiments, the principles involved are susceptible for use in numerous other embodiments which will be apparent to persons skilled in the art. The invention is, therefore, to be limited only as indicated by the scope of the appended claims.

Claims

1. In combination,

first means for providing standard interframe video signals,

second means for providing television signals,

third means for providing graphics signals,

fourth means for providing color palette signals,

fifth means for storing the signals from the first, second, third and fourth means,

sixth means for receiving the standard interframe video signals from the fifth means and for providing an output representative of such signals,

seventh means for receiving the television signals from the fifth means and for providing an output representative of such signals,

eighth means for receiving the graphics signals from the fifth means and for providing an output representative of such signals,

ninth means for providing a color palette having a plurality of positions each indicative of an individual color when selected,

tenth means for introducing the color palette signals from the fifth means to the individual positions in the color palette to obtain an indication of the individual colors at the individual positions in the color palette,

eleventh means for receiving the audio signals from the fifth means and for providing an output representative of such signals, and

twelfth means for activating an individual one of the sixth, seventh, eighth, tenth and eleventh means at each instant to obtain the transfer of signals from the fifth means to such individual one of the sixth, seventh, eighth, tenth and eleventh means at such instant.

2. In a combination as set forth in claim 1,

thirteenth means for providing a visual display in a raster scan defined by a plurality of lines, and

fourteenth means for storing the signals from the first through fifth means in each line in the raster scan in a particular sequence.

3. In a combination as set forth in claim 2,

the fourteenth means including fifteenth means for storing the signals from the first and third means in the fifth means for each line in the raster scan in timed synchronism with such line in the thirteenth means.

4. In a combination as set forth in claim 3,

each line in the raster scan by the thirteenth means having a blanking interval,

the fifteenth means including sixteenth means for initiating the storage of the signals from the first means in the fifth means for each line in the raster scan before the blanking interval in such line.

5. In a combination as set forth in claim 5,

the fifteenth means including seventeenth means for initiating the storage of the signals from the third means for each line in the raster scan during the blanking interval in such line, and

the fourteenth means including eighteenth means for storing the signals from the second and fourth means for each line in the raster scan in an asynchronous relationship in such line after the storage of the signals from the first and third means for the fifth means in such line.

6. In combination for use with a display monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels presented at a first particular frequency in each line,

storage means for storing bytes of graphics information and for providing for the transfer of such bytes of graphics information from the storage means at a second particular frequency greater than the first particular frequency,

shift register means for receiving the bytes of graphics information from the storage means at the second particular frequency and for simultaneously transferring the bytes of information from the shift register means at the first particular frequency,

a controller for providing for a transfer of the bytes of graphics information from the storage means to the shift register means at a particular time in each line, and

means responsive to the bytes of information shifted from the shift register means at the first particular frequency for converting such information to a form at the first particular frequency for display in the monitor.

7. In a combination as set forth in claim 5,

the shift register means having a capacity less than the number of bytes in each line in the raster scan in the monitor, and

the controller being operative to initiate the transfer of the bytes of graphics information from the storage means to the shift register means at a particular time in each line to provide for the introduction of the bytes of information for each line into the shift register means and to provide for a substantially full utilization of the shift register means in such line without any inability of the shift register means to receive bytes of graphics information for such line from the storage means.

8. In a combination as set forth in claim 6,

the shift register means constituting first shift register means,

the storage means being operative to store bytes of standard interframe video information,

second shift register means for receiving the bytes of the standard interface video information and for providing for the transfer of the bytes of the standard video information from the shift register means at the first particular frequency,

the controller being operative to provide for a selective transfer of the bytes of the standard interframe video information in the storage means to the second shift register

means at first particular times relative to each line and the bytes of the graphics information to the first shift register means at second particular times relative to each line,

the converting means being operative to convert the information in the second shift register means in each line in the raster scan to the form for display in the monitor, and

the controller being operative to provide for the conversion by the converter means of the successive bytes in the first shift register means for each line at third particular times and the successive bytes in the second shift register means for each line at fourth particular times different from the third particular times.

9. In a combination as set forth in claim 7,

there being a blanking interval in each line in the raster scan,

the shift register means constituting first shift register means,

the storage means being operative to store bytes of standard interframe video information for each line in the raster scan,

second shift register means for receiving the bytes of the standard interface video information for each line in the raster scan and for providing for the transfer of the bytes of standard video information from the shift register means for such line at the first particular frequency,

the controller being operative to provide for a selective transfer of the bytes of the standard interframe video information in the storage means to the second shift register means at first particular times relative to each line and the bytes of the graphics information to the first shift register means at second particular times relative to each line,

the converting means being operative to convert the bytes of the standard interframe video information in the second shift register means for each line to the form for display in the monitor, and

the controller being operative to provide for the conversion by the converter means of the successive bytes in the first shift register means for each line at third particular times and the successive bytes in the second shift register means for each line at fourth particular times different from the third particular times,

the controller being operative to initiate the transfer of the bytes of the standard interframe video information in the storage means to the second shift register means for each line at the second particular frequency at a particular time before the blanking interval in such line and to initiate the transfer of the bytes of the graphics information in the storage means to the first shift register means at the second particular frequency at a particular time for each line during the blanking interval in such line.

10. In a combination as set forth in claim 6,

the shift register means constituting first shift register means,

the storage means being operative to store bytes of at least a particular one of television information and audio information,

second shift register means for receiving the bytes of the at least one of the television information and the audio information in each line in the raster scan and for providing for the transfer of the bytes of the at least one of the television information and the audio information in each line from the second shift register means at the first particular frequency,

the controller being operative to provide for a selective transfer of the bytes of the graphics information in the storage means to the first particular shift register at a particular time relative to each line and the bytes of the at least one of the television information and the audio information to the second shift register means in each line after the transfer of the bytes of the graphics information relative to that line to the first shift register means.

11. In a combination as set forth in claim 10,

the controller being operative to provide for a transfer of the bytes of the at least one of the television information and the audio information in the storage means to the second shift register means at the second frequency on an asynchronous basis in each line without reference to any particular time in such line, after the transfer of the bytes of the graphics information relative to that line to the first shift register means at the particular time in such line.

12. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels presented at a first particular frequency in each line,

storage means for storing bytes of audio information and for providing for the transfer of the bytes of audio information from the storage means at a first particular frequency,

shift register means for receiving the bytes of audio information from the storage means and for transferring the bytes of audio information from the shift register means at the first particular frequency,

a controller for providing for a transfer of

the bytes of the audio information for each line from the storage means to the shift register means at the second particular frequency,

first means for providing a control signal when the shift register means has been filled for any particular line in the raster scan with the bytes of the audio information to a particular percentage of the capacity of the shift register means, and

second means responsive to the control signal for interrupting the transfer of the bytes of the audio information for such particular line from the storage means to the shift register means.

13. In a combination as set forth in claim 12,

the shift register means constituting first shift register means,

the storage means also storing bytes of graphics information for display on the video screen,

second shift register means for receiving the bytes of the graphics information from the storage means and for transferring the bytes of the graphics information from the second shift register means at the first frequency, and

third means for converting the bytes of the display information transferred from the second shift register means to a form for display on the monitor,

the controller providing for the transfer of the bytes of the display information from the storage means to the second shift register means at a particular time relative to each line.

14. In a combination as set forth in claim 13,

the means for converting the bytes of audio information constituting first converter means,

second converter means responsive to the bytes of the display information from the second shift register means for each line in the raster scan for converting such bytes to visual information,

the controller means being operative to activate the first converter means at first particular times and to selectively activate the second converter means at second particular times different from the first particular times.

15. In a combination as set forth in claim 14 wherein

a first bus extends from the controller to the storage means to provide the bytes of information for storage in the storage means and a second bus extends from the controller to the first and second shift register means to control the time for the transfer of the bytes of the display information from the storage means to the second shift register means and the selective activation of the first converter means at the first particular times and the second converter means at the second particular times.

16. In a combination as set forth in claim 2,

the shift register means being operative to receive the bytes of audio information at a second particular frequency greater than the first particular frequency.

17. In a combination as set forth in claim 13,

the first register means being operative to receive the bytes of audio information at a second particular frequency greater than the first particular frequency and the second register means being operative to receive the bytes of the graphics information from the storage means at the second particular frequency.

18. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels presented at a first particular frequency in each line,

storage means for storing bytes of television information and for providing for the transfer of the bytes of television information from the storage means at a first particular frequency,

shift register means for receiving the bytes of television information from the storage means and for transferring the bytes of television information from the shift register means at the first particular frequency,

a controller for providing for a transfer of the bytes of the television information for each line from the storage means to the shift register means at the second particular frequency,

means for providing a control signal when the shift register means has been filled for any particular line in the raster scan with the bytes of the television information to a particular percentage capacity of the shift register means, and

means responsive to the control signal for interrupting the transfer of the bytes of the television information from the storage means to the shift register means.

19. In a combination as set forth in claim 18,

the shift register means constituting first shift register means,

the storage means also storing bytes of graphics information for display on the monitor,

second shift register means for receiving

the bytes of graphics information from the storage means and for transferring the bytes of the graphics information from the second shift register means at the first frequency,

means for converting the bytes of the graphics information transferred from the second shift register means to a form for display on the monitor,

the controller providing for the transfer of the bytes of the graphics information from the storage means to the second shift register means at a particular time relative to each line in the raster scan.

20. In a combination as set forth in claim 19,

the means for converting the bytes of the graphics information constituting first converter means,

second converter means responsive to the bytes of the television information from the first shift register means for each line in the raster scan for converting such bytes to visual information, and

television means for displaying the visual information from the second converter means,

the controller means being operative to activate the first converter means at first particular times and to selectively activate the second converter means at second particular times different from the first particular times.

21. In a combination as set forth in claim 20 wherein

a first bus extends from the controller to the storage means to provide the bytes of information for storage in the storage means and a second bus extends from the controller to the first and second shift register means to control the time for the transfer of the bytes of the display information from the storage means to the second shift register means and the selective activation of the first and second converter means respectively at the first and second particular times.

22. In a combination as set forth in claim 18,

the shift register means being operative to receive the bytes of the television information at a second particular frequency greater than the first particular frequency.

23. In a combination as set forth in claim 19,

the first shift register means being operative to receive the bytes of the television information at a second particular frequency greater than the first particular frequency and the second shift register means being operative to receive the bytes of the graphics information at the second particular frequency.

24. In combination,

storage means for storing bytes of different types of digital information selected from a group including standard interface video information, graphics information, audio information and television information and for providing for a transfer of such different types of information from the storage means,

a plurality of shift register means each operative to receive and store the bytes of an individual one of the different types of digital information,

a plurality of first means each associated with an individual one of the shift register means in the plurality and operative to convert to analog form at the first particular frequency the bytes of digital information from the individual one of the shift register means in the plurality, and

controller means for providing for the transfer of each individual one of the different types of digital information in a particular sequence relative to each line in the raster scan, at a second particular frequency greater than the first particular frequency, to the individual one of the shift register means receiving that individual one of the different types of digital information, and

second means for transferring at each instant the bytes of information from a selective one of the shift register means to a selective one of the first means for the presentation in analog form of the information introduced to such selective one of the second means.

25. In a combination as set forth in claim 24 wherein

each byte having a plurality of bits,

the controller means and the storage means being operative to provide for the passage of the bits in each successive byte of the different types of digital information from the controller means to the storage means in parallel form and the storage means being operative to pass the bits in each successive byte of the different types of digital information from the storage means to the individual ones of the shift register means in serial form.

26. In a combination as set forth in claim 24 for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels in each line,

means including a first bus for providing for the transfer of the successive bytes of the

different types of digital information from the controller means to the storage means, and

means including a second bus for selecting the individual one of the shift register means to receive the successive bytes of digital information from the storage means at each instant and for synchronizing the reception by the individual ones of the shift register means of the bytes of the standard interface video information and graphics information for each line relative to the presentation of the successive lines in the raster scan in the monitor.

27. In a combination as set forth in claim 24 for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels in each line,

means including a first bus for providing for the transfer of the successive bytes of the different types of digital information from the controller means to the storage means, and

means including a second bus for selecting the individual ones of the shift register means in the plurality to receive the successive bytes of digital information from the storage means at each instant and for synchronizing the reception by such individual ones of the shift register means of the bytes of the standard interface video information and graphics information for each line with the presentation of the lines in the raster scan in the monitor,

each line in the raster scan in the monitor having a blanking interval at the beginning of each line,

means including the second bus for initiating the transfer of the bytes of the standard interframe video information for each line from the storage means to the individual one of the shift register means at a particular time before the blanking interval for such line in the raster scan, and

the shift register means for the bytes of the graphics information in each line having a capacity less than the number of bytes in such line of the graphics information and the means including the second bus initiating the transfer of the bytes of the graphics information for each line into the individual one of the shift register means at a time during the blanking interval in each line in the raster scan in the monitor to provide substantially full use of such shift register means in such line without preventing any transfer of the bytes of the graphics information into such shift register means throughout such line because of the full loading of such shift register means.

28. In a combination as set forth in claim 24 for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels in each line,

each line in the raster scan in the monitor having a blanking interval at the beginning of the line,

means including a bus for initiating the transfer of the bytes of the standard interface video information for each line, at a particular time before the blanking interval, from the storage means to the individual one of the shift register means receiving such bytes and for initiating the transfer of the bytes of the graphics information for each line, at a particular during the blanking interval in such line, from the storage means to the individual one of the shift register means receiving such bytes.

29. In a combination as set forth in claim 28,

the shift register means for the bytes of the graphics information having a capacity less than the number of bytes in each line of the graphics information and the controller means being operative to initiate the transfer of the bytes of the graphics information into such shift register means at a time during the blanking interval in each line in the raster scan in the monitor to provide substantially full use of such shift register means in such line without preventing any transfer of the bytes of the graphics information into such shift register means throughout such line because of the full loading of such shift register means.

30. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels presented at a first particular frequency in each line,

storage means for storing bytes of different types of digital information selected from a group including standard interframe video information, graphics information, audio information and television information and for providing for a transfer of such different types of information from the storage means,

a plurality of shift register means each operative to receive and store the bytes of an individual one of the different types of digital information and to pass such stored information from such shift register means,

a plurality of converter means each associated with an individual one of the shift register means in the plurality and each operative to convert to analog form the bytes of digital information from the associated one of the shift

register means in the plurality,

means for providing for the transfer of the bytes of at least a first one of the different types of information, at a particular time relative to each line in the raster scan in the monitor, from the storage means to a first individual one of the shift register means receiving such bytes, and

means for providing for the transfer of the bytes of at least a second one of the different types of information in each line, at times relative to such line after the transfer of the bytes of the first individual one of the different types of information to the first individual one of the shift register means in such line but without reference to any particular time relative to such line, from the storage means to a second individual one of the shift register means receiving such bytes.

31. In a combination as set forth in claim 30 wherein

the bytes of the first individual one of the different types of information are selected from the group including of standard interframe video information and graphics information and wherein

the bytes of the second individual one of the different types of information are selected from the group including audio information and television information.

32. In a combination as set forth in claim 30,

means for providing for the transfer of the bytes of a pair of the different types of information in each line in the raster scan, at particular times relative to such line in the raster scan in the monitor and in a particular order for the information in the pair of different types, from the storage means to a respective pair of the shift register means in the plurality.

33. In a combination as set forth in claim 32,

the pair of the different types of information constituting a first pair and the pair of the shift register means in the plurality constituting a first pair,

means for providing for the transfer of the bytes of a second pair of the different types of information in each line in the raster scan, in a particular order and at times after the transfer of the bytes of the first pair of the different types of information to the first respective pair of the shift register means but without reference to any particular time relative to such line, from the storage means to a second respective pair of the shift register means in the plurality.

34. In a combination as set forth in claim 32,

there being a blanking interval at the beginning of each line,

the means for providing for the transfer of the bytes of the pair of the different types of information relative to each line in the raster providing for such transfer at particular times in such line relative to the blanking interval in such line.

35. In a combination as set forth in claim 33,

the first pair of the different types of information constituting the standard interframe video information and the graphics information and the second pair of the different types of information constituting the television information and the audio information.

36. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels presented at a first particular frequency in each line,

storage means for storing bytes of different types of digital information, including standard interframe video information and graphics information, for each line in the raster scan in the monitor,

a plurality of shift register means each operative to receive and store the bytes of an individual one of the different types of information and to pass such stored information from such shift register means at the first particular frequency,

a plurality of converter means each associated with an individual one of the shift register means in the plurality and each operative to convert to analog form the bytes of digital information from the associated one of the shift register means in the plurality,

first means for transferring the bytes of the different types of digital information from the storage means to the individual ones of the shift register means at a second frequency greater than the first frequency, the first means being operative to initiate the transfer of such bytes for each line at a particular time relative to such line,

the shift register means for the standard interframe video information having a capacity corresponding to the bytes of digital information for supplying the pixels in each line,

the shift register means for the graphics information having a capacity less than that for providing the bytes for the pixels in each line,

the first means being operative to initiate the transfer of the bytes of graphics information for each line from the storage means to

the shift register means for such bytes at a time relative to such line to provide for the transfer of the bytes for such line into and out the shift register means before the end of such line without overloading the shift register means for such line and to provide for the use of substantially the full capacity of the shift register means in storing the bytes of information for such line.

37. In a combination as set forth in claim 36,

each of the lines in the raster scan in the monitor having a blanking interval at the beginning of such line,

the first means being operative to initiate the transfer of the bytes of the standard interframe video information from the storage means to the individual one of the shift register means for such bytes at a time for each line before the beginning of the blanking interval for that line.

38. In a combination as set forth in claim 36,

each of the lines in the raster scan in the monitor having a blanking interval at the beginning of such line,

there being more than one type of standard interframe video information for each line,

there being an individual one of the shift register means for each different type of standard interframe video information,

the first means being operative to initiate the transfer of the bytes of the different types of standard interframe video information to the individual ones of the shift register means for such bytes at a time for each line before the beginning of the blanking interval for such line,

the first means being operative to transfer the bytes of the different types of standard interframe video information to the individual ones of the shift register means for such bytes before the transfer of the bytes of the graphics information for such line to the shift register means receiving such bytes.

39. In a combination as set forth in claim 36,

the storage means also storing bytes of at least one of television information and audio information in digital form,

there being an individual one of the shift register means for the bytes of the at least one of the television information and the audio information,

the first means being operative to initiate the transfer of the bytes of the at least one of the television information and the audio information for each line from the storage means to the individual one of the shift register means for such bytes after the transfer of the bytes of the standard interframe video information and the graphics information for such line to the individual ones of the shift register means for such bytes, the first means being operative to initiate the transfer of the bytes of the at least one of the television information and audio information for such line without reference to any particular time in such line.

40. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels presented at a first particular frequency in each line,

storage means for storing bytes of digital graphics information and for providing for a transfer of such digital graphics information from the storage means at a second particular frequency greater than the first particular frequency,

shift register means for receiving and storing the bytes of the digital graphics information and for passing such information from the shift register means in the same order as the reception of such bytes by the shift register means, the shift register means having a capacity less than that for storing the bytes for a complete line of pixels,

means for converting the bytes of the digital graphics information from the shift register means at the first frequency into analog representations of such bytes, and

means for initiating the transfer of the bytes of the digital graphics information from the storage means into the shift register means at the second frequency at a time relative to each line to obtain the transfer of such bytes from the shift register means at the first frequency for such line without overloading the shift register means in such line.

41. In a combination as set forth in claim 40,

each line in the raster scan having a blanking interval,

the shift register means having a capacity, and the initiation of the transfer of the bytes of the digital graphics information from the storage means to the shift register means occurring at a time relative to the blanking interval in each line, to substantially fill the shift register means with such bytes during the transfer of such bytes into the shift register means in such line without overloading the shift register means in such line.

42. In a combination as recited in claim 41,

means for providing a control signal in

each line if and when the shift register means becomes full with the bytes of the digital graphics information in such line before the end of such line, and

means responsive to the control signal for interrupting the transfer of the digital graphics information from the storage means to the shift register means in such line.

43. In a combination as recited in claim 40,

means including a line for providing clock signals at the second particular frequency and for introducing such clock signals to the shift register means to provide for the transfer of the bytes of the digital graphics information from the storage means to the shift register means in synchronism with such clock signals, and

means including a bus for providing for the activation of the shift register means to receive the bytes of digital graphics information for each line at a particular time relative to the blanking interval in such line.

44. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels presented at a first particular frequency in each line,

storage means for storing bytes of digital standard interframe video information and for providing for a transfer of such information from the storage means at a second particular frequency greater than the first particular frequency,

shift register means for receiving and storing the bytes of the digital standard interframe video information and for passing such information from the shift register means in the same order as the reception of such bytes by the shift register means,

means for converting the bytes of the digital standard interframe video information from the shift register means at the first frequency into analog representations of such bytes, and

means for initiating the transfer of the bytes of the digital standard interframe video information into the shift register means at the second frequency at a time relative to each line to obtain the transfer of such bytes from the shift register means at the first frequency into such line.

45. In a combination as recited in claim 44,

each of the lines having a blanking interval,

means including a line for providing clock signals at the second particular frequency and for introducing such clock signals to the shift register means to provide for the transfer of the bytes of the digital standard interframe video information from the storage means to the shift register means in synchronism with the clock signals, and

means including a bus for providing for the activation of the shift register means to receive the bytes of digital standard interframe video information for each line at a particular time relative to the blanking interval in such line.

46. In a combination as set forth in claim 45,

the shift register means having a capacity for receiving the bytes of the digital standard interframe video information in each line, and

the means including the bus providing for the transfer of the bytes of the digital standard interframe video information for each line from the storage means to the shift register means before and during the blanking interval for such line.

47. In a combination as set forth in claim 45,

the bus providing a tag indicating in digital form the time for the initiation of the transfer of the bytes of the digital standard interframe signals from the storage means to the shift register means for each line, and

the means including the bus also including a state machine for decoding the tag to provide a synchronizing signal for initiating the transfer of the bytes of the digital standard interframe video information from the storage means to the shift register means for each line, and

means for initiating the transfer of the bytes of the digital standard interframe video information from the storage means to the shift register means in accordance with the provision of the synchronizing signal.

48. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels presented at a first particular frequency in each line,

storage means for providing bytes of digital information from a group of different types of information including standard interframe video information, graphics information, television information and audio information and for transferring such bytes from the storage means,

a plurality of shift register means each operative to receive and store the bytes of digital information from an individual one of the different types in the group and after a delay,

to transfer such bytes from such shift register means at the first particular frequency in the same order as received,

a plurality of converter means operative to receive the bytes of digital information from individual ones of the shift register means in the plurality and to produce analog signals representative of such bytes,

first means including a bus for providing digital signals indicating the individual one of the shift register means to be activated at each instant in the plurality to receive bytes of digital information from the storage means at the second particular frequency, and

second means responsive to the digital signals from the last mentioned means at each instant for selecting the individual one of the shift register means in the plurality to receive bytes of digital information from the storage means at that instant.

49. In a combination as set forth in claim 48,

the storage means being operative to transfer the bytes of the digital information from the storage means at a second particular greater than the first particular frequency.

50. In a combination as set forth in claim 48,

the means including the bus also including state machine means responsive to the signals on the bus for determining the order in which the bytes of the different types of information are to be transferred for each line to the individual ones of the shift register means in the plurality, and

the means for selecting the individual ones of the shift register means in the plurality being responsive to the determinations by the state machine means to receive the bytes of digital information of the type determined by the state machine means.

51. In a combination as set forth in claim 50,

the state machine means being responsive to the signals on the bus for determining for each line the times at which the bytes of individual ones of the different types of information are to be transferred from the storage means to the individual ones of the shift register means receiving such bytes.

52. In a combination as set forth in claim 51,

each line having a blanking interval at the beginning of the line,

the state machine means being responsive to the signals on the bus for initiating the transfer of the bytes of the digital standard interframe video information, at a particular time for each line before the blanking interval for that line, from the storage means to the individual one of the shift register means receiving such bytes and for initiating the transfer of the bytes of the digital graphics information, at a particular time for each line after the transfer of the bytes of standard interframe video information, from the storage means to the individual one of the shift register means receiving such bytes.

53. In combination,

storage means for holding bytes of different types of digital information selected from a group of standard interframe video information, graphics information, television information and audio information,

a plurality of shift register means each operative to receive and store the bytes of an individual one of the different types of digital information and to transfer such digital information from such shift register means in the same order as received,

an additional shift register means,

the storage means also holding additional bytes of digital information providing timing information and providing for the selective transfer at each instant of the bytes of digital information from the storage means in the plurality to the additional shift register means,

first means including a bus for activating the additional shift register means at particular times,

second means responsive to the activation of the additional shift register means for providing for the transfer of the additional bytes of digital information to the additional shift register means,

third means responsive to the additional bytes of digital information in the shift register means for decoding such information to provide timing signals and control signals providing for the selective transfer of the bytes of digital information from the individual ones of the shift register means in the plurality,

fourth means responsive to the timing signals and the control signals for obtaining a selective transfer of the bytes of digital information from the individual one of the shift registers in the plurality for each line, and

fifth means for processing the bytes of digital information selectively transferred from the individual ones of the shift register means in the plurality to convert such bytes to analog information.

54. In a combination as set forth in claim 53,

each additional byte having a plurality of

binary bits,

first bits in each additional byte providing the information for the production of the timing and control signals,

the third means being responsive to the first bits in the additional bytes for decoding such first bits to provide the timing signals and the control signals providing for the selective transfer of the bytes of digital information from the individual ones of the shift register means in the plurality,

sixth means for providing clock signals at a particular frequency,

second bits in the additional bytes being responsive to the clock signals for providing a count of the clock signals in each additional byte,

the fifth means being responsive to the count of the clock signals in the additional bytes and to the timing signals and the decoding signals in such additional bytes for processing the bytes of digital information selectively transferred from the individual ones of the shift register means in the plurality to convert such bytes to analog information.

55. In a combination as set forth in claim 53,

means responsive to the count of the clock signals in each additional byte for providing for the transfer of the bytes of the different types of digital information from the storage means into the individual ones of the shift register means in the plurality.

56. In a combination as set forth in claim 53,

a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels presented at a first particular frequency in each line, there being horizontal sync signals in each line in the raster scan and blanking signals in such line and vertical sync signals at the end of such raster scan,

the third means being responsive to the additional bytes of information for decoding such signals to provide the horizontal sync signals for such line and the blanking signals for such line and the vertical sync signals for such raster scan.

57. In a combination as set forth in claim 54,

each additional byte having a plurality of binary bits,

first bits in each additional byte providing the information for the production of the timing and control signals,

the third means being responsive to the first bits in the additional bytes for decoding such first bits to provide the timing signals and the control signals providing for the selective transfer of the bytes of digital information from the individual ones of the shift register means in the plurality,

sixth means for providing clock signals at a particular frequency,

second bits in the plurality being responsive to the clock signals for providing a count of the clock signals in each additional bytes,

the fifth means being responsive to the count of the clock signals and to the timing signals and the control signals for processing the bytes of digital information selectively transferred from the individual ones of the shift register means in the plurality to obtain analog information.

58. In combination,

first means for providing bytes of different types of digital information selected from a group including standard interframe video information, graphics information, television information and audio information,

a plurality of shift register means each operative to receive the bytes of an individual one of the different types of digital information,

an additional shift register means for receiving additional bytes of digital information indicative of timing and controls,

second means including a bus for providing for the selection of an individual one of the shift register means in the plurality or the additional shift register means,

the first means also providing bytes of digital information of an additional type for providing for the timing and transfer of the bytes of digital information from the individual ones of the shift register means in the plurality and the processing of such transferred bytes,

third means responsive to the selection by the second means of an individual one of the shift register means in the plurality or the additional shift register means for processing the bytes of the digital information received by such individual one of the shift register means in the plurality, and

fourth means responsive to the bytes of the digital information introduced to the additional shift register means for processing such bytes of digital information to obtain the selection of one of the shift register means in the plurality and the processing of the bytes of digital information in the selected one of the shift register means in the plurality in accordance with the timing and control information in the bytes in the additional shift register means.

59. In a combination as set forth in claim 58,

each of the additional bytes of digital information having a plurality of bits,

fifth means for providing clock signals at a particular frequency,

sixth means for providing a count of the clock signals to a value indicated by first bits in each additional byte, and

seventh means responsive to the count of the clock signals as provided by the sixth means for processing second bits in each additional byte to provide the timing and control for the processing of the bytes of digital information in the selected one of the shift register means in the plurality.

60. In a combination as set forth in claim 59,

eighth means for loading the bytes of each different type of digital information into the individual one of the shift register means at a second particular frequency greater than the first particular frequency, and

ninth means for synchronizing the loading provided by the eighth means in accordance with the count provided by the sixth means.

61. In a combination as set forth in claim 58,

a plurality of eighth means each associated with an individual one of the shift register means in the plurality for processing the bytes of digital information in such individual one of the shift register means in the plurality, the eighth means associated with the shift register means for the standard interframe video information and the graphics information being operative in synchronism with the clock signals.

62. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels in each line,

storage means having a plurality of positions each storing indications in binary form of the intensity of each of three primary colors,

first means responsive to the selection of any individual one of the positions in the storage means for converting to analog form the indications of each of the three (3) primary colors at such position,

second means for selecting for each of the pixels in each line in the raster scan in the monitor an individual one of the positions in the storage means for display at such pixel of an image in accordance with the intensity at such position in the storage means of each of the three primary colors, and

third means operative at the end of each raster scan for updating the indications of the three (3) primary colors at each of the positions in the storage means.

63. In a combination as set forth in claim 62,

each raster scan providing for a vertical retrace at the end of each raster scan,

the third means being operative during the vertical retrace in each raster scan to update the indications of the primary colors at each of the positions in the storage means.

64. In a combination as set forth in claim 63,

the monitor being operative to present the pixels in each line at a first particular frequency,

the second means including shift register means for receiving and storing bytes of binary information for each line in the raster scan in the monitor and for transferring such bytes of information from the shift register means in the same order as received by the shift register means, and

the third means further including fourth means for transferring into the shift register means the bytes of binary information, at a second frequency greater than the first frequency, to provide for an updating of the indications of the three (3) primary colors at the different positions in the storage means during the vertical retrace period.

65. In combination as set forth in claim 62,

means including a bus for providing indications of the times when the bytes of binary indications are to be transferred into the shift register means and for activating the fourth means at such times and for providing indications of the times when the different positions in the storage means are to be updated by the bytes of binary indications in the shift register means and the third means are to provide such updating.

66. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels presented in each line at a first particular frequency,

first storage means for storing bytes indicative of different types of binary information selected from a group including standard interframe video information, graphics information, television information and audio information,

second storage means providing a plurality of positions each storing in binary form indications of the three binary indications cumulatively indicating a color for the graphics in-

formation,

a plurality of shift register means each operative to receive and store bytes of an individual one of the different types of binary information and to transfer such bytes from such shift register means in the same order as received by such shift register means,

first means for transferring the bytes indicative of the different types of binary information, in a particular order in each line in the raster scan in the monitor, into the shift register means in the plurality at a second particular frequency greater than the first particular frequency,

second means for selecting in each line an individual one of the shift register means in the plurality to transfer from the shift register means the bytes in such shift register means, and

third means for transferring into each position in the second storage means at the end of each raster scan, from the particular one of the shift register means receiving the bytes of graphics information, the indications representing an updated color for such position in the second storage means.

67. In a combination as set forth in claim 66,

an additional shift register means for indicating the times for the transfer of the bytes of the different ones of the types of binary indications into the different ones of the shift registers in the plurality,

fourth means for transferring at particular times into the additional shift register means from the first storage means the bytes of binary indications providing the information for the times for the transfer of the different types of binary indications into the different ones of the shift register means in the plurality,

the first means being responsive to the indications from the additional shift register means for transferring the bytes indicative of the different ones of the types of binary indications into the different ones of the shift register means at the times indicated by the additional shift register means.

68. In a combination as set forth in claim 67,

fifth means including a bus for activating the fourth means to provide a transfer at the particular times into the additional shift register means from the first storage means of the bytes of binary indications providing the information for the times for the transfer of the different types of binary indications into the individual ones of the shift register means in the plurality.

69. In a combination as set forth in claim 66,

fifth means for processing the bytes of the binary indications transferred from individual ones of the shift register means in the plurality, and

sixth means for obtaining the processing by the fifth means of the bytes of binary indications passing from the individual ones of the shift register means in the plurality.

70. In a combination as set forth in claim 67,

fifth means for processing the bytes of the binary indications transferred from the individual ones of the shift register means in the plurality, and

sixth means responsive to the indications from the additional shift register means for obtaining the processing by the fifth means of the bytes of binary indications passing from the individual ones of the shift register means in the plurality.

71. In a combination as set forth in claim 66,

the raster scan in the monitor having a vertical retrace period at the end of each raster scan, and

fourth means including a bus for activating the third means during the vertical retrace in each raster scan to obtain a transfer by the third means into the second storage means of the indications representing an updated color for each position in the second storage means, these indications being obtained from the individual one of the shift register means receiving the bytes of graphics information.

72. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels presented in each line at a first particular frequency,

storage means for storing bytes of different types of digital information selected from a group including standard interframe video information, graphics information, television information and audio information,

a plurality of shift register means each operative to receive and store the bytes of an individual one of the different types of digital information and to transfer such bytes from such shift register means in the same order as received by such shift register means,

first means for transferring the bytes of the different types of digital information into the shift register means in the plurality at a second particular frequency higher than the first particular frequency,

second means including a bus for indicat-

ing at each instant the individual one of the shift register means from which digital information is to be transferred at each instant, and

a plurality of decoding means each operatively coupled to an individual one of the shift register means in the plurality and each responsive to the indications from the second means to activate such individual one of such shift register means in the plurality in accordance with the indications from the second means to transfer the bytes of digital information from the individual one of the shift register means.

73. In a combination as set forth in claim 72,

the storage means being operative to store the bytes of an additional one of the different types of digital information,

an additional shift register means operative to receive and store the bytes of the additional one of the different types of digital information and to transfer such bytes from such shift register means in the same order as received by such shift register means,

the second means also indicating the additional shift register means to receive the bytes being transferred from the storage means,

the additional bytes of digital information indicating the timing for the transfer of the bytes of the different types of digital information from the individual ones of the shift register means in the plurality, and

third means responsive to the additional bytes of digital information in the additional shift register means for timing the transfer of the bytes of the different types of digital information from the individual ones of the shift register means in the plurality into the individual ones of the decoding means in the plurality.

74. In a combination as set forth in claim 72,

the second means including the bus indicating at each instant the individual one of the shift register means to receive the bytes of digital information being transferred from the storage means at that instant, and

the first means being responsive to the indications from the second means for transferring the bytes of the individual types of the digital information into the individual one of the shift register means in the plurality at the second particular frequency.

75. In a combination as set forth in claim 73,

the additional bytes of digital information also indicating the timing for the transfer of the individual types of digital information into the individual ones of the shift register means in the plurality at the second particular frequency,

the first means being responsive to the timing indications from the second means for transferring the bytes of the individual types of the digital information into the individual ones of the shift register means in the plurality at the second particular frequency.

76. In a combination as set forth in claim 66,

the third means being operative to transfer at the first frequency at each instant the bytes of digital information from the individual ones of the shift register means in the plurality at such instant.

77. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels in each line,

first means for providing bytes of different types of digital information selected from a group including standard interframe video information, graphics information, television information and audio information,

storage means for storing the different types of digital information,

second means for introducing into the storage means, in parallel form, the bytes of the different types of digital information,

a plurality of shift register means each operative to receive and store the bytes of an individual one of the different types of digital information and to transfer such bytes from the shift register means in the same order as received, and

third means for serially transferring into the individual ones of the shift register means in the plurality, in a particular order for each line, the bytes of the different types of information for such line.

78. In a combination as set forth in claim 77,

the pixels in each line in the raster scan in the monitor being presented at a first particular frequency,

the third means being operative to transfer the bytes of the individual ones of the different types of digital information into the individual ones of the shift register means in the plurality at a second particular frequency greater than the first particular frequency.

79. In a combination as set forth in claim 78,

there being a blanking interval at each line in the raster scan in the monitor, and

fourth means for obtaining the transfer by the third means into the individual ones of the

shift register means in the plurality of the bytes of the individual ones of the different types of digital information at particular times with respect to each line related to the blanking interval in such line.

80. In a combination as set forth in claim 77 wherein

each line in the raster scan in the monitor has a blanking interval at the beginning of each line and wherein

fourth means are included for providing for the transfer of the bytes of the digital standard interframe video information into the associated one of the shift register means in the plurality at a particular time for each line before the blanking interval for that line and for providing for the transfer of the bytes of the digital graphics information into the associated one of the shift register means in the plurality at a particular time for each line after the transfer of the bytes of the digital standard interframe video information into the shift register means.

81. In a combination as set forth in claim 80,

the fourth means being operative to transfer the bytes of other ones of the different types of digital information from the storage means into the associated ones of the shift register means in the plurality in each line after the transfer of the bytes of the individual ones of the digital standard interframe video information and digital graphics information into the shift register means in the plurality in such line and to provide such transfer without reference to any particular time in such line.

82. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels in each line,

storage means for storing bytes of different types of digital information selected from a group including standard interframe video information, graphics information, television information and audio information,

a plurality of shift register means such operative to receive and store an individual one of the different types of digital information and to transfer such digital information from such shift register means in the same order as received,

first means for providing a transfer in a particular order of the bytes of the different types of digital information from the storage means into the individual ones of the shift register means for each line in the raster scan in the monitor,

the storage means also storing bytes of digital cursor information,

an additional register means for receiving and storing the bytes of the digital cursor information and for transferring the bytes from the additional shift register means in the same order as received, and

second means for providing the transfer of the bytes of the digital cursor information into the additional shift register means for a particular line in the raster scan in the monitor.

83. In a combination as set forth in claim 74,

each line in the raster scan in the monitor having a blanking interval,

third means for providing a transfer in each line in the raster scan of the bytes in individual ones of the different types of digital information from the storage means into the individual ones of the shift register means in the plurality in a particular time relationship to the blanking interval in such line and for providing a transfer of the bytes of the digital cursor information from the storage means into the additional shift register means for the particular line in each raster scan at a particular time for each line relative to the transfer of the different types of digital information from the storage means into the individual ones of the shift register means in the plurality.

84. In a combination as set forth in claim 82,

the third means being operative to transfer the bytes of digital information from the storage means into the shift register means in the plurality at a second particular frequency greater than the first particular frequency.

85. In a combination as set forth in claim 82,

third means for processing the bytes of digital information transferred from the shift register means in the plurality and the additional shift register means,

fourth means for providing binary indications controlling the transfer at each instant of the bytes of digital information from a selective one of the shift register means in the plurality and the additional shift register means into the third means, and

fifth means responsive to the binary indications from the fourth means for transferring the bytes of digital information from the selective one of the shift register means and the additional shift register means into the third means.

86. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels in each line,

storage means for providing bytes of different types of digital information selected from a group including standard interframe video information, graphics information, television information and audio information,

a plurality of shift register means each operative to receive and store an individual one of the different types of digital information and to transfer such digital information in the same order as received and stored,

first means for transferring the digital information in the storage means to the shift register means in the plurality,

second means for providing tags for the bytes of digital information transferred from the storage means to the shift register means in the plurality, each tag being indicative of the individual one of the shift register means to which a byte of digital information in the storage means is to be transferred, and

third means responsive to the tags from the second means for providing for the transfer of the bytes of digital information by the first means from the storage means to the individual ones of the shift register means in the plurality in accordance with the indication in the tags of such individual ones of the shift register to receive such bytes.

87. In a combination as set forth in claim 86,

the third means including fourth means for decoding the tag and further including additional shift register means for receiving and storing the decoded information and for transferring the decoded information from the additional shift register means,

the third means also including fifth means responsive to the decoded information from the fourth means for activating the individual ones of the shift register means to receive the bytes of digital information from the storage means.

88. In a combination as set forth in claim 86,

the pixels in each line in each raster scan in the monitor being presented at a first particular frequency,

the first means being operative to transfer the bytes of the digital information in the storage means to the shift register means in the plurality at a second particular frequency greater than the first particular frequency.

89. In a combination as set forth in claim 86,

the fifth means providing for the transfer of first individual ones of the different types of digital information, at particular times relative to each line in each raster scan in the monitor, to first individual ones of the shift register means receiving such bytes in the plurality and providing for the transfer of second individual ones of the different types of digital information, after the bytes of the first individual ones of the bytes of digital information relative to such line and without reference to any particular times in such line, to second individual ones of the shift register means receiving such bytes in the plurality.

90. In a combination as set forth in claim 89,

sixth means for processing the bytes of digital information transferred from the shift register means in the plurality,

the fifth means being operative to select at each instant the particular one of the shift register means in the plurality to transfer bytes of digital information to the sixth means for processing by the sixth means.

91. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels in each line,

controller means for providing bytes of the different types of digital information selected from a group including standard video information, graphics information, television information and audio information,

storage means for storing bytes of the different types of digital information transferred from the controller means,

a plurality of shift register means each operative to receive and store the bytes of an individual one of the different types of digital information and to transfer such bytes from such individual one of the shift register means in the same order as received by such shift register means,

first means for transferring the bytes of the different types of digital information between the controller means, the storage means and individual ones of the shift register means in the plurality,

second means in the controller means for providing digital information indicating the path for the transfer of the bytes of the different types of digital information between the individual ones of the controller means, the storage means and the individual ones of the shift register means in the plurality, and

third means for providing a transfer of the

different types of digital information between the individual ones of the controller means, the storage means and the individual ones of the shift register means in the plurality in accordance with the digital information from the second means.

92. In a combination as set forth in claim 91 wherein
the storage means includes a dynamic random access memory.

93. In a combination as set forth in claim 91,
the second means including fourth means for providing a tag bus indicating in binary coded form the path for the transfer of the bytes of the different types of digital information between the controller means, the storage means and the individual ones of the shift register means in the plurality, and
the third means including fifth means for decoding the coded information in the fourth means to provide the transfer of the bytes of the different types of digital information between the storage means, the controller means and the individual ones of the shift register means in the plurality in accordance with such decoding.

94. In a combination as set forth in claim 92,
means in the controller means for addressing the storage means to obtain the transfer of the bytes of the different types of digital information between the controller means and the storage means.

95. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels in each line,
controller means for providing bytes of different types of digital information selected from a group including standard interframe video information, graphics information, television information and audio information,
storage means for receiving and storing the bytes of the different types of digital information and for transferring such bytes from the storage means,
a plurality of shift register means each operative to receive and store the bytes of the different types of digital information and for transferring such bytes from the storage means in the same order as received,
first means including a first bus extending from the controller means for addressing the storage means with respect to the transfer of bytes of digital information between the controller means and the storage means,
second means including a second bus for providing digital information for the transfer of the bytes of the different types of digital information between the controller means, the storage means and the individual ones of the shift register means in the plurality, and
third means responsive to the information from the second means for providing digital instructions controlling the transfer of the bytes of the different types of digital information between the controller means, the storage means and the individual ones of the shift register means in the plurality.

96. In a combination as set forth in claim 95,
the third means including fourth means for decoding the digital information in the second means,
the third means including fifth means responsive to the decoded digital information from the fourth means for providing for the transfer, at particular times for each line in each raster scan in the monitor, of the bytes of individual ones of the different types of digital information from the storage means to the individual ones of the shift register means in the plurality receiving such bytes.

97. In a combination as set forth in claim 96,
the third means including sixth means responsive to the decoded digital instructions for providing for the transfer, after the transfer of the bytes of the individual ones of the different types of digital information from the storage means for each line but without any reference to any particular time relative to such line, of the bytes of second particular ones of the different types of digital information from the storage means to the individual ones of the shift register means in the plurality receiving such bytes.

98. In a combination as set forth in claim 97,
each of the lines having a blanking interval at the beginning of the line,
the fifth means being operative to transfer, at particular times for each line relative to the blanking interval in such line, the bytes of the individual ones of the different types of digital information to the individual ones of the shift register means in the plurality.

99. In a combination as set forth in claim 98,
the pixels in each line being presented at a particular clock frequency,
the sixth means being operative to introduce to the controller means a synchronizing

signal for each line, and

the sixth means including seventh means for providing for the transfer of the bytes of the individual ones of the different types of digital information from the shift register means in the plurality at a particular time in each line and at the particular clock frequency.

100. In a combination as set forth in claim 99,

the pixels in each line being presented at a particular clock frequency,

the third means being operative to introduce to the controller means a synchronizing signal for each line,

the third means being operative to provide for the transfer of the bytes of individual ones of the different types of digital information from the shift register means in the plurality at a particular time for each line and at the particular clock frequency,

the individual one of the shift register means in the plurality for the graphics information having a capacity to store a number of bytes less than the number of pixels in each line,

the sixth means being operative to initiate the transfer of the bytes of digital information into such individual one of the shift register means t a particular time for each line to provide a substantially full, but less than full, utilization of the capacity of such shift register means in such line.

101. In a combination as set forth in claim 100,

the third means being operative to transfer the bytes of the digital television information and the digital audio information into the individual ones of the shift register means for each line on a basis unrelated to any time in the line but after the transfer for such line of the graphics information into the shift register means receiving such graphics information.

102. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels in each line,

controller means for providing bytes of different types of digital information selected from a group including standard interframe video information, graphics information, television information and audio information,

storage means for receiving and storing the bytes of the different types of digital information and for transferring such bytes from the storage means,

a plurality of shift register means each operative to receive and store the bytes of an individual one of the different types of digital information and for transferring such bytes from the shift register means in the same order as received,

first means including a first bus extending from the controller means to the storage means to address the storage means to provide a controlled transfer of the bytes of digital information into and out of the storage means,

second means including a second bus extending between the controller means, the storage means and the shift register means in the plurality for transferring the bytes of the different types of digital information between the controller means and the storage means and from the controller means and the storage means to the shift register means in the plurality, and

third means including a third bus for providing a controlled transfer of the bytes of the individual ones of the different types of digital information to the individual ones of the shift register means receiving such bytes.

103. In a combination as set forth in claim 102,

the storage means constituting at least one dynamic RAM.

104. In a combination as set forth in claim 102,

the third bus providing additional bytes of digital information providing for the selective transfer of the bytes of the individual ones of the different types of digital information in each line in the raster scan into the individual ones of the shift register means in the plurality,

the third means including means for decoding the additional bytes of digital information,

the third means including additional shift register means for receiving and storing the decoded bytes from the decoding means and for transferring such decoded bytes from the additional shift register means in the same order as received,

the third means including timing state means for operating upon the decoded bytes to obtain the controlled transfer of the bytes of the individual ones of the different types of digital information to the individual ones of the plurality of shift register means receiving such bytes.

105. In a combination as set forth in claim 104,

the timing state means providing for the transfer of the bytes of standard interframe video and graphics information at particular times for each line in the raster scan to the individual ones of the shift register means re-

ceiving such bytes and providing for the transfer of the bytes of television and audio information for each line in the raster scan to the individual ones of the shift register means receiving such bytes such that such transfer of the bytes of the television information and the audio information occurs for each line after the transfer of the standard video information and graphics information for such line but without reference to any particular time.

106. In a combination as set forth in claim 105,

the pixels in each line in the raster scan being presented at a particular clock frequency,

the storage means constituting a dynamic RAM,

the third means being operative to transfer the bytes of the different types of digital information to the shift register means in the plurality at the particular clock frequency.

107. In a combination as set forth in claim 102,

the individual ones of the shift register means for the bytes of television information and audio information having limited capacities,

means for providing a control signal when the individual ones of the shift register means for the bytes of television information and audio information become filled for any line in the raster scan by the transfer of the bytes of the television and audio information into such shift register means, and

means interrupting the transfer of the bytes of the television and audio information into such individual ones of the shift register means for such line upon the production of the control signal in such line.

108. In a combination as set forth in claim 102,

each of the bytes of digital information being formed from a plurality of bits,

the second means being operative to transfer the bits in each byte in parallel between the controller means and the storage means and from the controller means and the storage means to the shift register means in the plurality.

109. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels generated in each line,

controller means for providing bytes of different types of digital information selected from a group including standard interframe video information, graphics information, television information and audio information,

storage means for storing the bytes of the different types of digital information,

a plurality of shift register means each operative to receive and store the bytes of digital information for an individual one of the different types of digital information and to transfer such bytes from such shift register means in the same order as received,

a bus extending between the controller means, the storage means and the shift register means in the plurality and providing successive bytes of digital information representing data and other bytes of digital information representing the destination of such data among the controller means, the storage means and the shift register means in the plurality, and

first means for directing the individual ones of the bytes of digital information from the storage means to the individual ones of the shift register means in the plurality in accordance with the information in such other ones of such bytes.

110. In a combination as set forth in claim 109,

each of the other ones of the bytes including a plurality of bits, first ones of which indicate that second bits in such bytes contain information indicating the destination of successive ones of the individual bytes,

the first means including second means responsive to the first bits in the other bytes for decoding the second bits in such bytes and for directing the successive ones of the individual bytes to the individual ones of the shift register means in the plurality in accordance with such decoding.

111. In a combination as set forth in claim 109,

the second bits in the other bytes providing digital information indicating the timing of the transfer, for each line in the raster scan in the monitor, of the bytes of individual ones of the different types of digital information into the individual ones of the shift register means in the plurality receiving such individual ones of the different types of digital information, and

the first means including third means responsive to the digital information indicating such timing for directing successive ones of the individual bytes to such individual ones of the shift register means in the plurality in accordance with such timing.

112. In a combination as set forth in claim 111,

the pixels in each line in the raster scan in the monitor being presented at a first frequen-

cy,

the shift register means for the graphics information having a capacity less than that for storing the bytes for all of the pixels in each line,

the graphics information being transferrable into the shift register means for the graphics information at a second clock frequency greater than the first clock frequency, and

the third means being operative to initiate the transfer of the bytes of the graphics information into the shift register means for such graphics information at a time for each line to substantially but not completely fill such shift register means for such line.

113. In a combination as set forth in claim 111,

the pixels in each line in the raster scan in the monitor being presented at a first frequency,

the shift register means for an individual one of the television and audio information having a capacity less than that for storing the bytes for all of the pixels in each line,

the bytes for the individual one of the television and audio information being transferrable into the individual one of the shift register means for such information at a second frequency greater than the first frequency,

the third means being operative to transfer the bytes of such individual one of the television information and the audio information into such individual one of the shift register means for each line but without any particular timing for such line, and

fourth means for interrupting the transfer of the bytes of such individual one of the television information and audio information into such shift register means for each line when the shift register means becomes filled to a particular capacity for such line.

114. In combination for use with a monitor for displaying information, the monitor providing a raster scan defined by a plurality of lines and by a plurality of pixels in each line,

controller means for providing bytes of different types of digital information selected from a group including standard interframe video information, graphics information, television information and audio information,

storage means for storing the bytes of the different types of digital information,

a plurality of shift register means each operative to receive and store the bytes of digital information and to transfer such bytes from such shift register means in the same order as received,

a bus extending between the controller means, the storage means and the shift register means in the plurality and providing successive bytes first ones of which provide the individual ones of the different types of digital information and second ones of which indicate the individual ones of the shift register means in the plurality to receive the successive bytes after such second ones of the bytes and also providing indications controlling the processing of the indications in such successive bytes, each of the bytes having a particular bit indicating whether such byte constitutes one of the first ones or one of the second ones of the bytes,

first means for processing the bytes in the individual ones of the shift register means in the plurality,

second means responsive to the particular bit in each byte for determining whether such byte constitutes one of the first bytes or one of the second bytes,

third means responsive to the determination by the second means for decoding the byte when the determination is that the byte constitutes one of the second bytes, and

fourth means responsive to the decoding provided by the third means for one of the second bytes for passing the successive bytes to an individual one of the shift register means in the plurality in accordance with such decoding.

115. In a combination as set forth in claim 114,

the shift register means in the plurality for the graphics information having a capacity less than the number of pixels in each line in the raster scan in the monitor, and

means for initiating the transfer of the bytes of the graphics information from the storage means into the shift register means in the plurality for such graphics information at a particular time in each line to provide for a substantially full, but not an overflowing, use of the capacity of the shift register means in such line.

116. In a combination as set forth in claim 115,

means for initiating the transfer of the bytes of the standard interframe video information into the shift register means in the plurality for such standard interframe video information at a particular time in each line before the transfer in such line of the bytes of the graphics information into the shift register means in the plurality for such graphics information.

117. In a combination as set forth in claim 115,

means for initiating the transfer of the bytes of the television information and the audio information into the shift register means in the plurality for such information at a time in each line after the transfer of the graphics information in such line into the shift register means for such graphics information but without any reference to any particular time in such line.

118. In a combination as set forth in claim 117,

the shift register means in the plurality for at least one of the television information and the audio information having limited capacities,

means responsive to an overflow of the capacity in the shift register means for the at least one of the television information and the audio information for one of the lines in the raster scan for producing a control signal, and

means responsive to the control signal for discontinuing the transfer of the bytes for such line of the at least one of the television information and the audio information into the shift register means receiving such bytes.

119. In a combination as set forth in claim 114,

the storage means constituting at least one dynamic RAM.

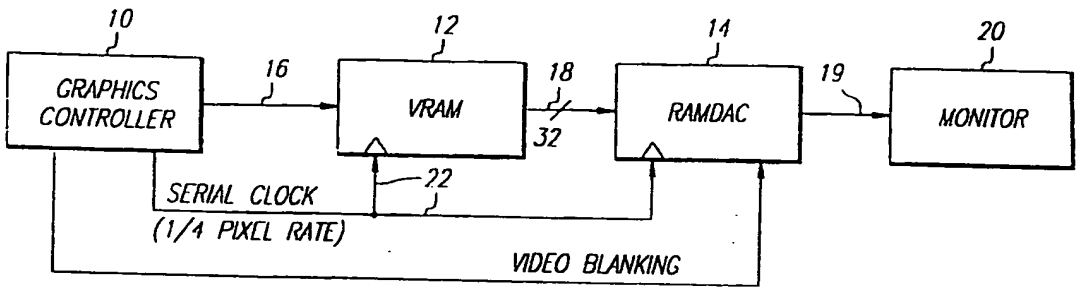

FIG. 1

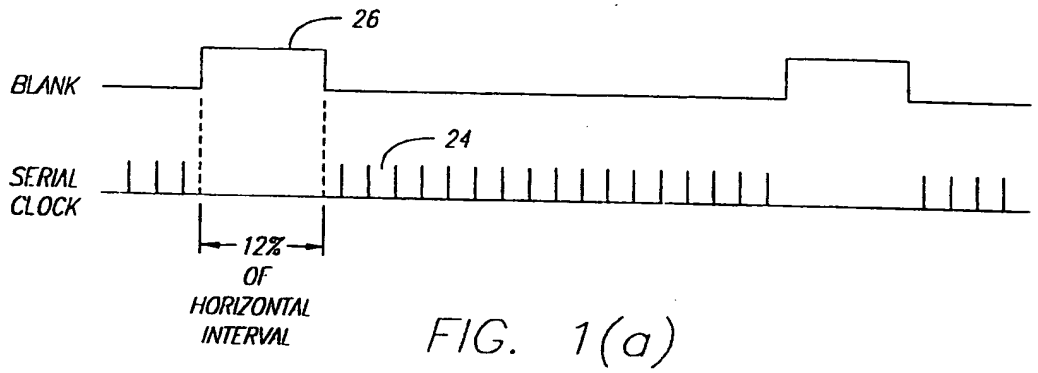

FIG. 1(a)

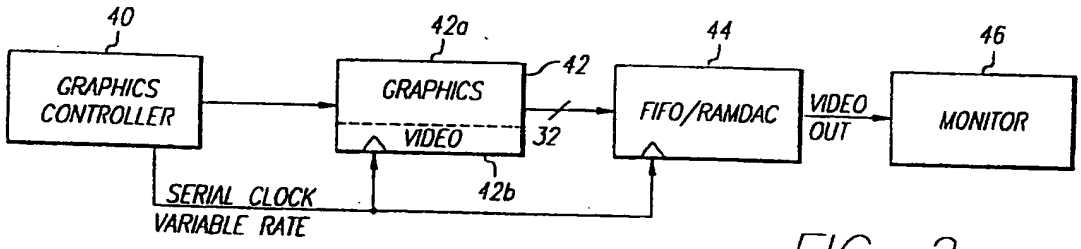

FIG. 2

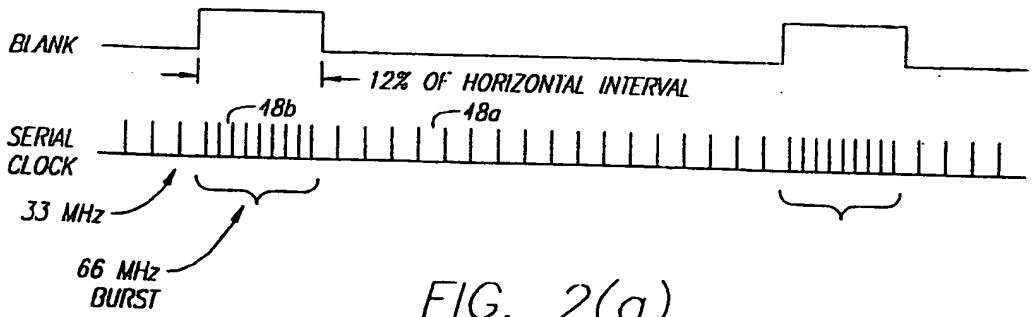

FIG. 2(a)

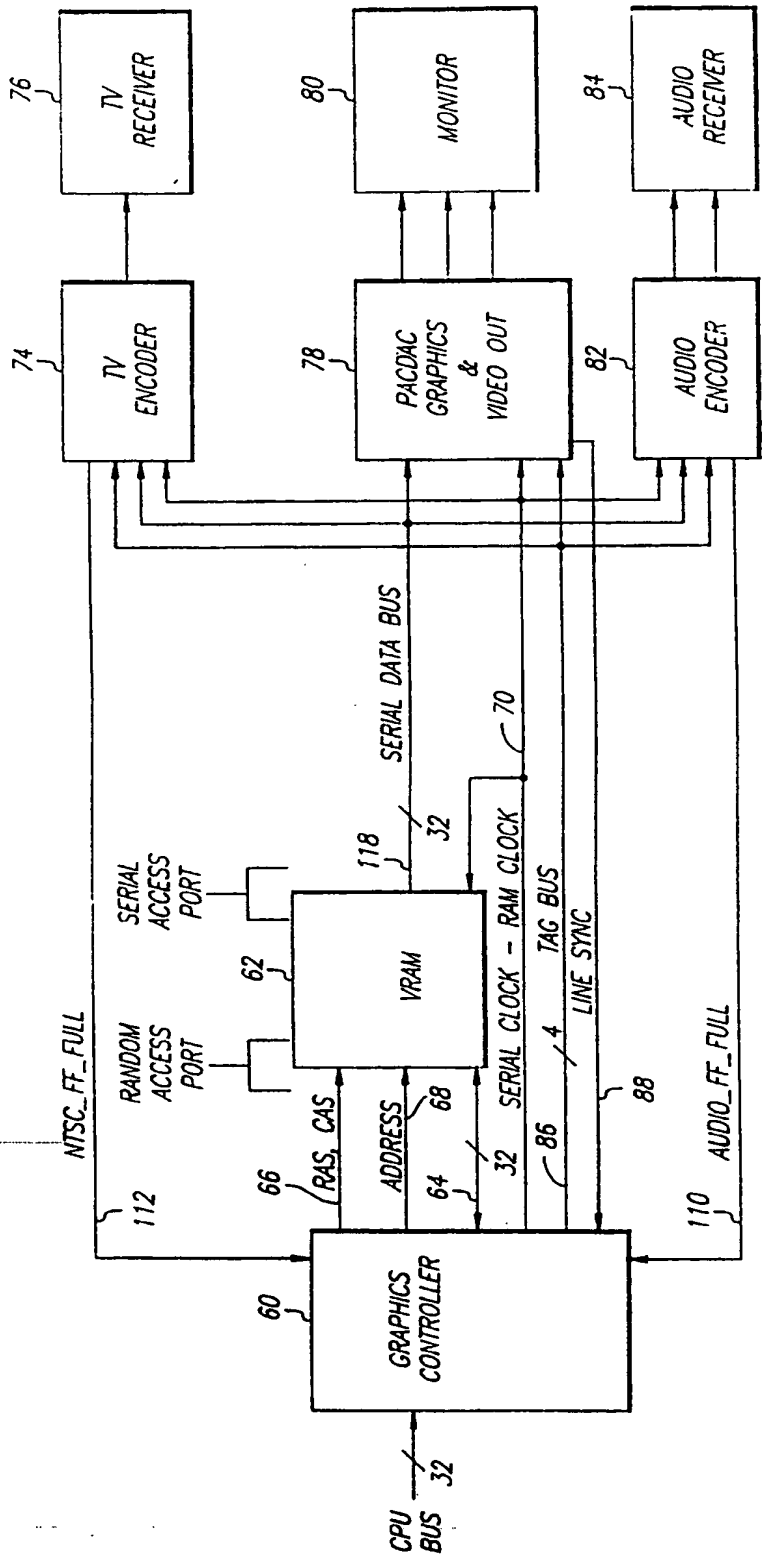
76
TV RECEIVER
80
MONITOR
84
AUDIO RECEIVER
74
TV ENCODER
78
PACDAC GRAPHICS & VIDEO OUT
82
AUDIO ENCODER
SERIAL DATA BUS
118
32
70
SERIAL ACCESS PORT
62
VRAM
RANDOM ACCESS PORT
SERIAL CLOCK - RAM CLOCK
TAG BUS
LINE SYNC
4
NTSC_FF_FULL
112
66
RAS, CAS
ADDRESS
68
64
32
86
88
AUDIO_FF_FULL
110
60
GRAPHICS CONTROLLER
CPU BUS
32

FIG. 3

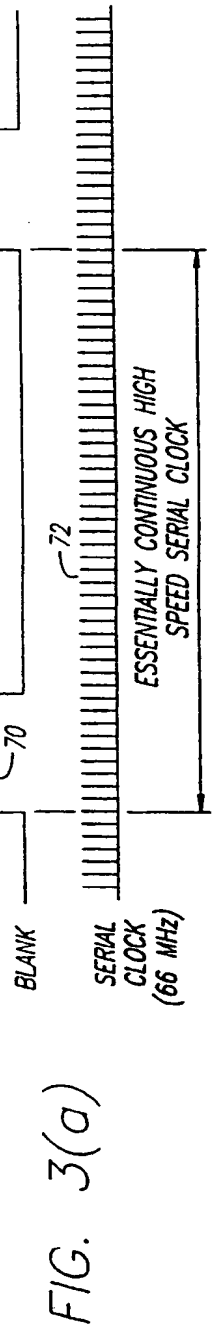
70
72
ESSENTIALLY CONTINUOUS HIGH SPEED SERIAL CLOCK
BLANK
SERIAL CLOCK (66 MHz)

FIG. 3(a)

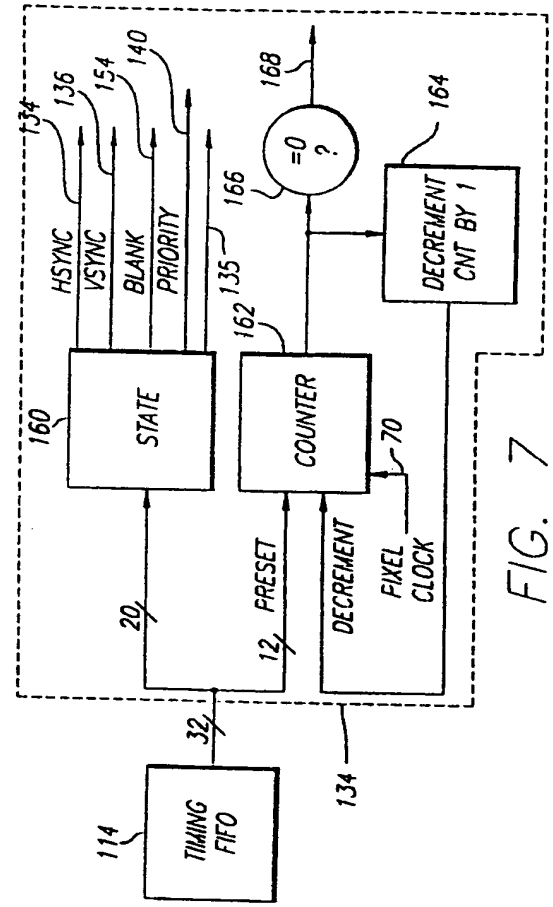

FIG. 4

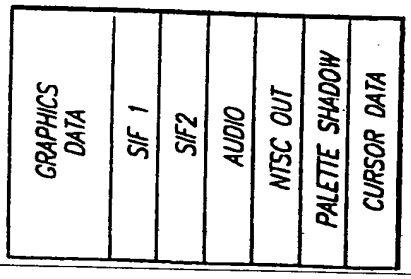

FIG. 7

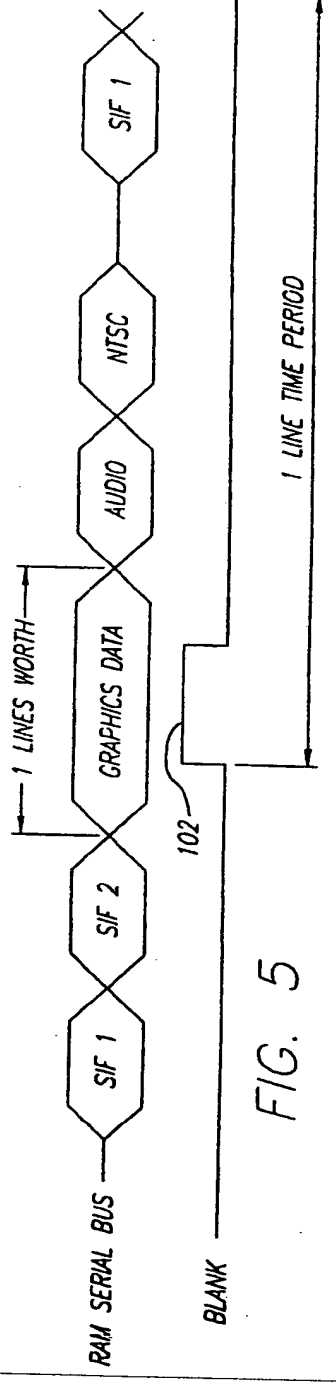

FIG. 5

FIG. 5(a)

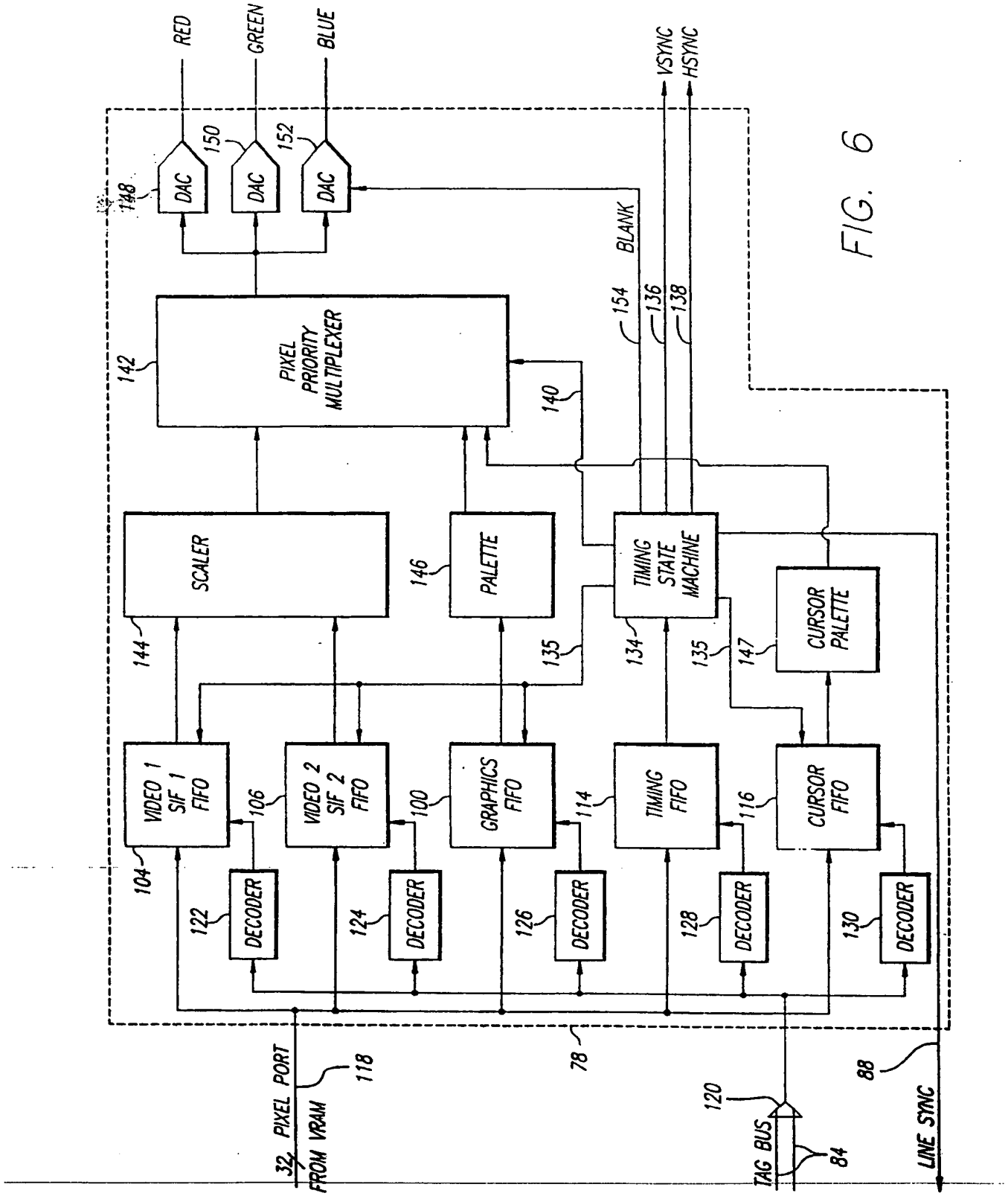

FIG. 6

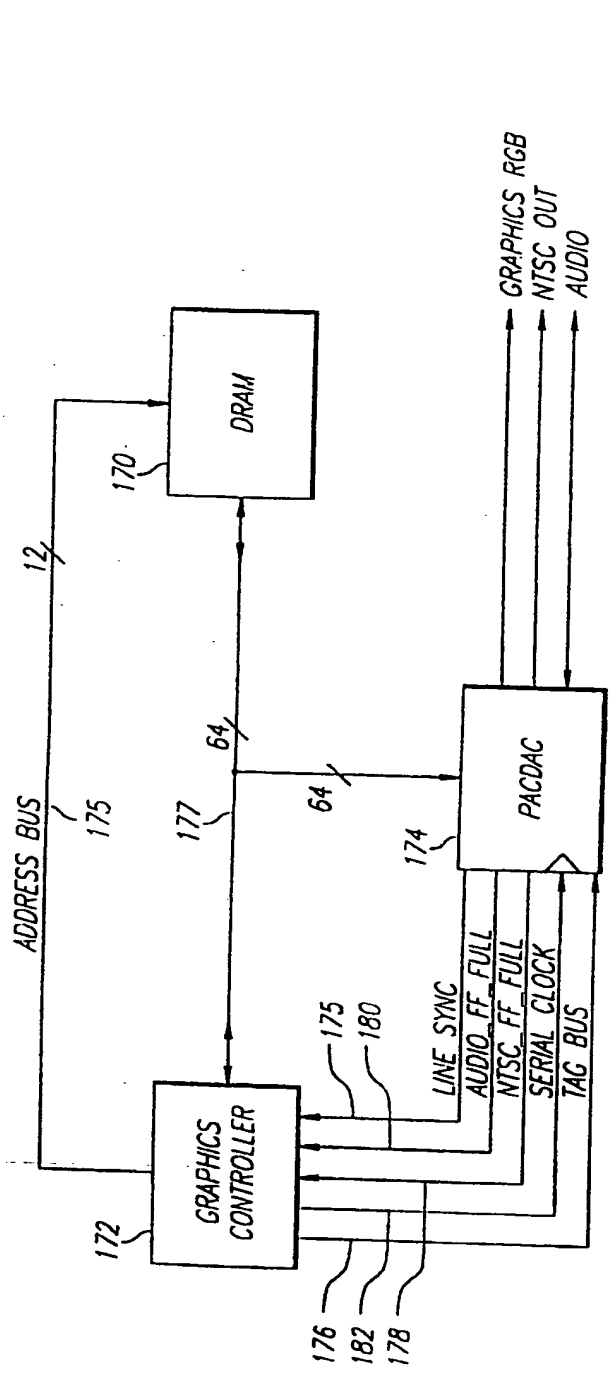
DRAM
170
12
ADDRESS BUS
175
177
64
64
PACDAC
174
GRAPHICS RGB
NTSC OUT
AUDIO
175
180
LINE SYNC
AUDIO_FF_FULL
NTSC_FF_FULL
SERIAL_CLOCK
TAG BUS
GRAPHICS CONTROLLER
172
176
182
178

FIG. 8

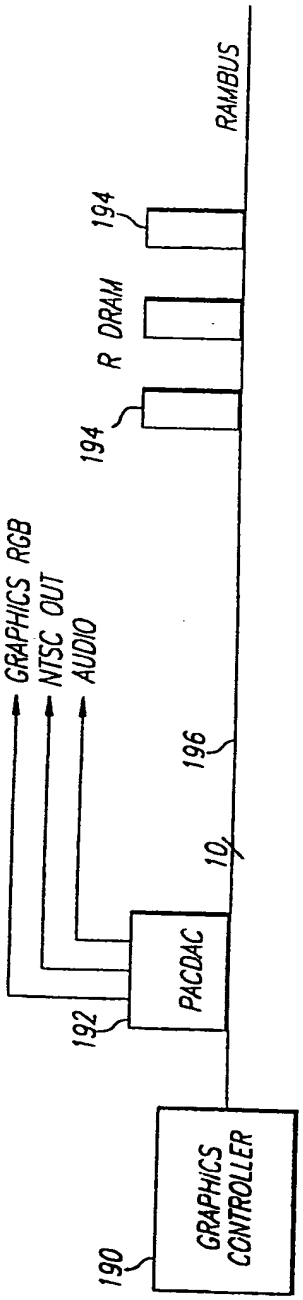
RAMBUS
194
R DRAM
194
GRAPHICS RGB
NTSC OUT
AUDIO
196
10
PACDAC
192
GRAPHICS CONTROLLER
190

FIG. 9

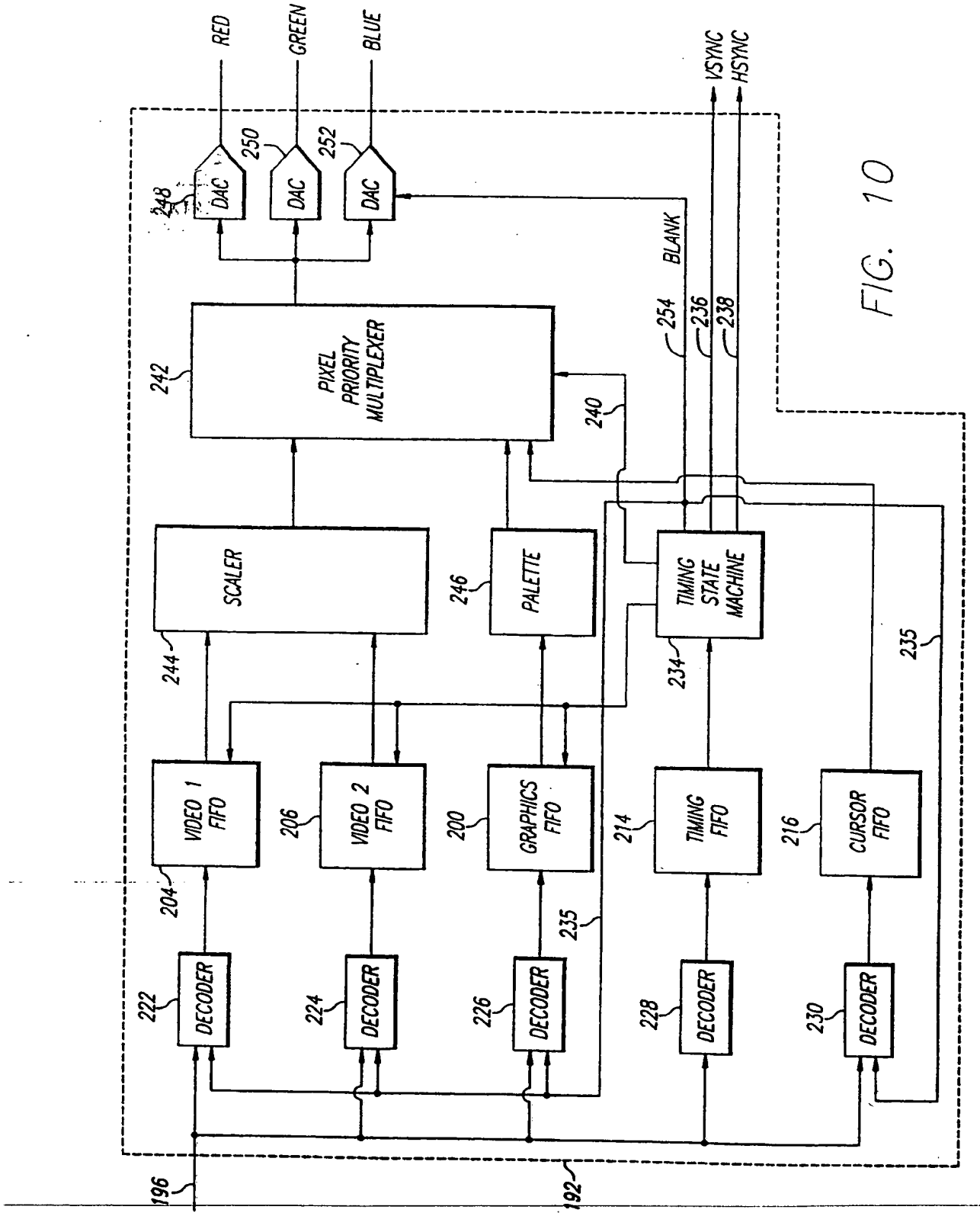

FIG. 10

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 10 2037

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
D,A, P	EP-A-0 610 829 (BROOKTREE CO.)		G09G1/16 G09G5/00
A	EP-A-0 454 414 (SONY CORPORATION OF AMERICA)		
P,A	EP-A-0 597 218 (INTERNATIONAL BUSINESS MACHINES CO.)		
P,A	EP-A-0 601 647 (PHILIPS ELECTRONICS N.V.)		
A	EP-A-0 524 468 (INTERNATIONAL BUSINESS MACHINES CO.)		
A	EP-A-0 493 881 (INTERNATIONAL BUSINESS MACHINES CO.)		
A	EP-A-0 492 795 (INTERNATIONAN BUSINESS MACHINES CO.)		
A	WO-A-93 21574 (VIDEOLOGIC LTD.)		TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 34, no. 10b, March 1992 NEW YORK US, pages 119-121, XP 000302599 'Utilization of motion detection information for system resource management in a multi media environment.'		G09G
A	ELEKTRONIK, vol. 41, no. 26, 22 December 1992 MUNCHEN DE, pages 32-38, XP 000327406 N. HUTH 'Rennstrecke für Bildschirmpixel 1. Teil'		

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18 July 1995	Farricella, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 10 2037

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	ELEKTRONIK, vol. 42, no. 1, 12 January 1993 MUNCHEN DE, pages 50-54, XP 000330965 N. HUTH 'Rennstrecke für Bildschirmpixel 2. Teil' -----		

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18 July 1995	Farricella, L

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X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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